

# BLUETECHNIX Embedding Ideas

## TIM-UP – 19k-S3-Spartan 6 V2.1.0

Software User Manual

Version 7





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#### Information

For further information on technology, delivery terms and conditions and prices please contact Bluetechnix (http://www.bluetechnix.com).

#### Warning

Due to technical requirements components may contain dangerous substances.





Last change: 9 January 2015 Version 7

## **1** General Information

This guide applies to the TIM<sup>uP</sup> - 19k-S3-Spartan6 module from Bluetechnix GmbH. Follow this guide chapter by chapter to set up and understand your product. If a section of this document only applies to certain camera parts, this is indicated at the beginning of the respective section.

#### 1.1 Symbols Used

This guide makes use of a few symbols and conventions:



#### Warning

Indicates a situation which, if not avoided, could result in minor or moderate injury and/or property damage or damage to the device.



#### Caution

Indicates a situation which, if not avoided, may result in minor damage to the device, in malfunction of the device or in data loss.

|  | 1 |  |
|--|---|--|
|  |   |  |

#### Note

Notes provide information on special issues related to the device or provide information that will make operation of the device easier.

#### Procedures

A procedure always starts with a headline

1. The number indicates the step number of a certain procedure you are expected to follow. Steps are numbered sequentially.

This sign ➤ indicates an expected result of your action.

#### References

This symbol indicates a cross reference to a different chapter of this manual or to an external document.



## 2 Overview

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The TIM<sup>uP</sup>-19k-S3-Spartan6 module is a Time-of-Flight Imaging Module with a resolution of 160 x 120 Pixels. It is designed to provide depth imaging data for any controller equipped with an USB Host interface, a Camera Sensor Interface (CSI) or an Image Sensor Module (ISM) interface. For easy access via USB, an powerful SDK is provided.

This document describes the necessary steps and settings to work with the TIM<sup>uP</sup> - 19k-S3-Spartan6 module and describes the firmware dependent interfaces.

#### This document applies to firmware version v2.1.0

For a hardware compatibility list please refer to our support site.

#### Software and documentation

https://support.bluetechnix.at/wiki/TIM-UP-19k-S3-Spartan6



## 3 Hardware Connector

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The following table shows the pin-out of the 100-pin TIM connector:

| Pin # | Туре | Signal name | Description  |
|-------|------|-------------|--|
| 1     |      | ISM.nDE     | ISM Output enable: 0: ISM bus enabled, 1: ISM bus high Z |
| 2     | NC   |             |  |
| 3     | NC   |             |  |
| 4     | NC   |             |  |
| 5     | NC   |             |  |
| 6     | PWR  | GND         | Power ground   |
| 7     | 0    | ISM.D7      | ISM Data Bit 7 (MSB)                                     |
| 8     | 0    | ISM.D6      | ISM Data Bit 6   |
| 9     | 0    | ISM.D5      | ISM Data Bit 5   |
| 10    | 0    | ISM.D4      | ISM Data Bit 4   |
| 11    | PWR  | GND         | Power ground   |
| 12    | NC   |             | 5  |
| 13    | 0    | ISM.D3      | ISM Data Bit 3   |
| 14    | 0    | ISM.D2      | ISM Data Bit 2   |
| 15    | 0    | ISM.D1      | ISM Data Bit 1   |
| 16    | 0    | ISM.D0      | ISM Data Bit 0 (LSB)                                     |
| 17    | 0    | TRIGGER.OUT | Trigger output signal: rising edge after LED modulation  |
| 18    | 1    | TRIGGER.IN  | Trigger input signal: trigger on rising edge             |
| 19    | 0    | ISM.HSYNC   | ISM Line Sync (HSYNC)                                    |
| 20    | 0    | ISM.VSYNC   | ISM Frame Sync (VSYNC)                                   |
| 21    | 0    | ISM.PCLK    | ISM Pixel clock  |
| 22    | PWR  | GND         | Power ground   |
| 23    | NC   |             |  |
| 24    | I/O  | ISM.SDA     | ISM Configuration bus data signal                        |
| 25    |      | ISM.SCL     | ISM Configuration bus clock signal                       |
| 26    | 1    | nRESET      | Reset signal: hardware reset on low                      |
| 27    | NC   |             |  |
| 28    | 1    | ISM.SADDR   | ISM Slave address (currently not supported)              |
| 29    | PWR  | GND         | Power ground   |
| 30    | NC   |             |  |
| 31    | NC   |             |  |
| 32    | PWR  | GND         | Power ground   |
| 33    | NC   |             |  |
| 34    | NC   |             |  |
| 35    | PWR  | GND         | Power ground   |
| 36    | NC   |             |  |
| 37    | NC   |             |  |
| 38    | PWR  | GND         | Power ground   |
| 39    | NC   |             |  |
| 40    | NC   |             |  |
| 41    | PWR  | GND         | Power ground   |
| 42    | NC   |             |  |
| 43    | NC   |             |  |
| 44    | NC   |             |  |
| 45    | NC   |             |  |
| 46    |      | UART.RX     | UART Receive   |



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| 47       O       UART.TX       UART Transmit         48       NC  | Pin # | Туре | Signal name | Description  |
|---|-------|------|-------------|--|
| 49       NC         50       NC         51       0       LED.SMOD       LIM Single ended mod signal         52       I/O       LED.IO       LIM one-wire communication bus (currently not supported)         53       PWR       GND       Power ground         54       0       LED.MOD_N       LIM Differential pair mod signal – positive         56       PWR       GND       Power ground         57       0       GPIO.3       GPIO 3: status signal (toggle on every frame capture)         58       -       Factory Default Reset: 4sec on low while reboot to delete register map from flash and boot delault configuration         59       I       GPIO.1       GPIO 1: not used – internal pull up         60       NC       -       -         61       NC       -       -         62       NC       -       -         63       PWR       GND       Power ground       -         64       NC       -       -       -         65       NC       -       -       -         66       NC       -       -       -         71 <th>47</th> <th></th> <th></th> <th>UART Transmit</th>   | 47    |      |             | UART Transmit  |
| 50       NC         51       O       LED.SMOD       LIM Single ended mod signal         52       I/O       LED.IO       LIM one-wire communication bus (currently not supported)         53       PWR       GND       Power ground         54       O       LED.MOD_N       LIM Differential pair mod signal - negative         55       O       LED.MOD_P       LIM Differential pair mod signal - positive         56       PWR       GND       Power ground         57       O       GPIO.3       GPIO 3: status signal (toggle on every frame capture)         58       -       register map from flash and boot default configuration         59       I       GPIO.1       GPIO 1: not used - nitemal pull up         60       NC       -       -         61       NC       -       -         63       PWR       GND       Power ground       -         64       NC       -       -         65       NC       -       -         66       NC       -       -         71       PWR       GND       Power ground         72  | 48    | NC   |             |  |
| 51       O       LED.SMOD       LIM Single ended mod signal         52       I/O       LED.IO       LIM one-wire communication bus (currently not supported)         53       PWR       GND       Power ground         54       O       LED.MOD_N       LIM Differential pair mod signal – negative         55       O       LED.MOD_P       LIM Differential pair mod signal – negative         56       PWR       GND       Power ground         57       O       GPIO.3       GPIO 3: status signal (toggle on every frame capture)         58       I       GPIO.2       Factory Default Reset: 4sec on low while reboot to delete register map from flash and boot default configuration         59       I       GPIO.1       GPIO 1: not used – internal pull up         60       NC   | 49    | NC   |             |  |
| 52       I/O       LED.IO       LIM one-wire communication bus (currently not supported)         53       PWR       GND       Power ground         54       O       LED.MOD_N       LIM Differential pair mod signal – negative         55       O       LED.MOD_P       LIM Differential pair mod signal – negative         56       PWR       GND       Power ground         57       O       GPIO.3       GPIO 3: status signal (toggle on every frame capture)         1       GPIO.3       GPIO 3: status signal (toggle on every frame capture)         6       PWR       GND       Power ground         60       NC       -       -         61       NC       -       -         63       PWR       GND       Power ground         64       NC       -       -         65       NC       -       -         66       NC       -       -         67       NC       -       -         68       PWR       GND       Power ground       -         71       PWR       GND       Power ground       -         74   | 50    | NC   |             |  |
| 53       PWR       GND       Power ground         54       O       LED.MOD_N       LIM Differential pair mod signal – negative         55       O       LED.MOD_P       LIM Differential pair mod signal – negative         56       PWR       GND       Power ground         57       O       GPIO.3       GPIO.3: status signal (toggle on every frame capture)         1       GPIO.2       Eactory Default Reset: 4sec on low while reboot to delete register map from flash and boot default configuration         59       I       GPIO.1       GPIO.1       GPIO.1         61       NC   | 51    | 0    | LED.SMOD    |  |
| 64       O       LED.MOD_N       LIM Differential pair mod signal – negative         55       PWR       GND       Power ground         57       O       GPI0.3       GPIO 3: status signal (togele on every frame capture)         58       -       register map from flash and boot default configuration         59       I       GPIO.1       GPIO 1: not used – internal pull up         60       NC       -       -         61       NC       -       -         62       NC       -       -         63       PWR       GND       Power ground       -         64       NC       -       -       -         65       NC       -       -       -         66       NC       -       -       -         67       NC       -       -       -         70       NC       -       -       -         71       PWR       GND       Power ground       -         72       NC       -       -       -         74       I       PEN       Module power enable       - <th>52</th> <th>I/O</th> <th>LED.IO</th> <th>LIM one-wire communication bus (currently not supported)</th>  | 52    | I/O  | LED.IO      | LIM one-wire communication bus (currently not supported) |
| 55       O       LED.MOD_P       LIM Differential pair mod signal – positive         56       PWR       GND       Power ground         57       O       GPIO.3       GPIO 3: status signal (toggle on every frame capture)         1       GPIO.1       GPIO 3: status signal (toggle on every frame capture)         58  | 53    | PWR  | GND         |  |
| 56       PWR       GND       Power ground         57       O       GPIO.3       GPIO 3: status signal (toggle on every frame capture)         1       GPIO.2       Factory Default Reset: 4sec on low while reboot to delete register map from flash and boot default configuration         59       I       GPIO.1       GPIO 1: not used – internal pull up         60       NC       61       NC         61       NC       62       NC         63       PWR       GND       Power ground         64       NC       65       NC         66       NC       66       NC         67       NC       68       PWR       GND         68       PWR       GND       Power ground       68         69       NC       70       NC       71         70       NC       72       NC       73         73       NC       74       I       PEN       Module power enable         75       NC       77       I/O       SPI.SCLK       Not used – high Z         77       I/O       SPI.SIO       Not used – high Z       73  | 54    |      |             | , , ,  |
| 57       O       GPIO.3       GPIO.3 is status signal (toggle on every frame capture)         I       GPIO.2       Factory Default Reset: 4sec on low while reboot to delete<br>register map from flash and boot default configuration         59       I       GPIO.1       GPIO 1: not used – internal pull up         60       NC  | 55    |      |             |  |
| I       GPIO.2       Factory Default Reset: Asec on low while reboot to delete register map from flash and boot default configuration         59       I       GPIO.1       GPIO 1: not used – internal pull up         60       NC       GPIO.1       GPIO 1: not used – internal pull up         61       NC       GPIO.1       GPIO 1: not used – internal pull up         62       NC       GRID       Power ground         63       PWR       GND       Power ground         64       NC       GRID       Forward 1: not used - internal pull up         66       NC       GRID       Power ground       GRID         66       NC       GRID       Power ground       GRID         70       NC       Total reset with the reset of t | 56    |      |             |  |
| 58       registor map from flash and boot default configuration         59       I       GPIO.1       GPIO 1: not used – internal pull up         60       NC         61       NC         62       NC         63       PWR       GND       Power ground         64       NC         65       NC         66       NC         67       NC         68       PWR       GND       Power ground         69       NC         70       NC         71       PWR       GND       Power ground         72       NC         73       NC       T         74       I       PEN       Module power enable         75       NC       T         76       O       SPI.SICIX       Not used – high Z         77       I/O       SPI.SICI       Not used – high Z         77       I/O       SPI.SICI       Not used – high Z         78       I/O       SPI.SICI       Not used – high Z         79       O       SPI.NCS       Not used – high Z  | 57    | 0    |             |  |
| 59       I       GPIO.1       GPIO 1: not used - internal pull up         60       NC   |       | I    | GPIO.2      |  |
| 60       NC         61       NC         62       NC         63       PWR       GND       Power ground         64       NC         65       NC         66       NC         67       NC         68       PWR       GND       Power ground         69       NC         70       NC         71       PWR       GND       Power ground         72       NC         73       NC         74       I       PEN       Module power enable         75       NC         76       O       SPLSUK       Not used - high Z         77       VO       SPLSU0       Not used - high Z         78       I/O       SPLSU1       Not used - high Z         79       O       SPLINCS       Not used - high Z         79       O       SPLINCS       Not used - high Z         81       NC       S       S         82       NC       S       S         84       NC       S       S <t< th=""><th></th><th></th><th></th><th></th></t<>   |       |      |             |  |
| 61       NC         62       NC         63       PWR       GND       Power ground         64       NC         65       NC         66       NC         67       NC         68       PWR       GND       Power ground         69       NC   |       | •    | GPIO.1      | GPIO 1: not used – internal pull up                      |
| 62     NC       63     PWR     GND     Power ground       64     NC       65     NC       66     NC       67     NC       68     PWR       69     NC       70     NC       71     PWR       63     NC       74     I       75     NC       76     O       77     I/O       78     I/O       79     O       78     I/O       79     O       79     O       79     O       79     O       70     NC       81     NC       82     NC       83     PWR       6ND     Power ground       84     NC       85     NC       86     NC       87     NC       88     PWR       6ND     Power ground       84     NC       85     NC       86     NC   |       |      |             |  |
| 63       PWR       GND       Power ground         64       NC   |       |      |             |  |
| 64       NC         65       NC         66       NC         67       NC         68       PWR         69       NC         70       NC         71       PWR         72       NC         73       NC         74       I         75       NC         76       O         77       I/O         78       I/O         79       O         78       I/O         78       I/O         79       O         78       I/O         79       O         80       NC         81       NC         82       NC         83       PWR         6ND       Power ground         84       NC         85       NC         86       NC         87       NC         88       PWR         6ND       Power ground         89       I/O         90       I/O   |       |      |             | Dower ground   |
| 65       NC         66       NC         67       NC         68       PWR       GND         70       NC         71       PWR       GND         72       NC         73       NC         74       I       PEN         75       NC         76       O       SPI.SCLK         77       I/O       SPI.SIOO         78       I/O       SPI.SIO         79       O       SPI.SIO         79       O       SPI.SIO         80       NC         81       NC         82       NC         83       PWR         GND       Power ground         84       NC         85       NC         86       NC         87       NC         88       PWR         GND       Power ground         89       I/O         90       I/O         91       NC         92       NC         93       O  |       |      | GND         | Power ground   |
| 66       NC         67       NC         68       PWR       GND       Power ground         69       NC         70       NC         71       PWR       GND       Power ground         72       NC         73       NC       T         74       I       PEN       Module power enable         75       NC       T         76       O       SPI.SCLK       Not used - high Z         77       I/O       SPI.SIO0       Not used - high Z         77       I/O       SPI.SIO1       Not used - high Z         78       I/O       SPI.SIO1       Not used - high Z         79       O       SPI.NCS       Not used - high Z         80       NC       E       E         81       NC       E       E         83       PWR       GND       Power ground         84       NC       E       E         85       NC       E       E         86       NC       E       E         90       I/O       <  |       |      |             |  |
| 67       NC         68       PWR       GND       Power ground         69       NC       Power ground         70       NC       Power ground         71       PWR       GND       Power ground         72       NC       Particular       Power ground         73       NC       Particular       Particular         74       I       PEN       Module power enable         75       NC       Particular       Particular         76       O       SPI.SCLK       Not used – high Z         77       I/O       SPI.SIO       Not used – high Z         78       I/O       SPI.SIO1       Not used – high Z         79       O       SPI.NCS       Not used – high Z         79       O       SPI.NCS       Not used – high Z         81       NC       Power ground       Power ground         84       NC       Power ground       Power ground         84       NC       Power ground       Power ground         89       I/O       USB.D_N       USB D- Signal: high Z on reset         90  |       |      |             |  |
| 68       PWR       GND       Power ground         69       NC   |       |      |             |  |
| 69       NC         70       NC         71       PWR       GND       Power ground         72       NC         73       NC         74       I       PEN       Module power enable         75       NC         76       O       SPI.SCLK       Not used - high Z         77       I/O       SPI.SIO0       Not used - high Z         78       I/O       SPI.SIO1       Not used - high Z         79       O       SPI.NCS       Not used - high Z         79       O       SPI.NCS       Not used - high Z         80       NC       S       S         81       NC       S       S         82       NC       S       S         83       PWR       GND       Power ground         84       NC       S       S         86       NC       S       S         87       NC       S       S         89       I/O       USB.D_N       USB D- Signal: high Z on reset         90       I/O       USB.D_P       USB D+ Signa  |       |      |             | Dower ground   |
| 70       NC         71       PWR       GND       Power ground         72       NC       PEN       Module power enable         73       NC       Module power enable       PEN         74       I       PEN       Module power enable         75       NC       Module power enable       Presson         76       O       SPI.SCLK       Not used – high Z         77       I/O       SPI.SIO1       Not used – high Z         78       I/O       SPI.SIO1       Not used – high Z         79       O       SPI.nCS       Not used – high Z         80       NC       Sector       Sector         81       NC       Sector       Sector         83       PWR       GND       Power ground         84       NC       Sector       Sector         86       NC       Sector       Sector         87       NC       Sector       Sector         88       PWR       GND       Power ground       Sector         89       I/O       USB.D_N       USB D- Signal: high Z on reset       Sector </th <th></th> <th></th> <th>GND</th> <th>Power ground</th>   |       |      | GND         | Power ground   |
| 71       PWR       GND       Power ground         72       NC   |       |      |             |  |
| 72     NC       73     NC       74     I     PEN     Module power enable       75     NC       76     O     SPI.SCLK     Not used – high Z       77     I/O     SPI.SIO0     Not used – high Z       78     I/O     SPI.SIO1     Not used – high Z       79     O     SPI.SIO1     Not used – high Z       79     O     SPI.NCS     Not used – high Z       80     NC     S     Not used – high Z       81     NC     S     Not used – high Z       82     NC     S     Not used – high Z       83     PWR     GND     Power ground       84     NC     S     S       85     NC     S     S       86     NC     S     S       87     NC     S     S       88     PWR     GND     Power ground       89     I/O     USB.D_N     USB D- Signal: high Z on reset       90     I/O     USB.D_P     USB D+ Signal: high Z on reset       91     NC     S     S <th></th> <th></th> <th></th> <th>Dowor ground</th>   |       |      |             | Dowor ground   |
| 73     NC       74     I     PEN     Module power enable       75     NC       76     O     SPI.SCLK     Not used – high Z       77     I/O     SPI.SIO0     Not used – high Z       78     I/O     SPI.SIO1     Not used – high Z       79     O     SPI.NCS     Not used – high Z       80     NC     S     Not used – high Z       81     NC     S     Not used – high Z       82     NC     S     Not used – high Z       83     PWR     GND     Power ground       84     NC     S     NC       85     NC     S     S       86     NC     S     S       87     NC     S     S       88     PWR     GND     Power ground       89     I/O     USB.D_N     USB D- Signal: high Z on reset       90     I/O     USB.D_N     USB D+ Signal: high Z on reset       91     NC     S     S       92     NC     S     S       93     O     I2CM.SCL<   |       |      | GIND        | Fower ground   |
| 74     I     PEN     Module power enable       75     NC       76     O     SPI.SCLK     Not used – high Z       77     I/O     SPI.SIO0     Not used – high Z       78     I/O     SPI.SIO1     Not used – high Z       79     O     SPI.nCS     Not used – high Z       80     NC   |       |      |             |  |
| 75       NC         76       O       SPI.SCLK       Not used - high Z         77       I/O       SPI.SIO0       Not used - high Z         78       I/O       SPI.SIO1       Not used - high Z         79       O       SPI.nCS       Not used - high Z         80       NC       Sector       Sector         81       NC       Sector       Sector         82       NC       Sector       Sector         83       PWR       GND       Power ground         84       NC       Sector       Sector         85       NC       Sector       Sector         86       NC       Sector       Sector         87       NC       Sector       Sector         88       PWR       GND       Power ground       Sector         89       I/O       USB.D_N       USB D- Signal: high Z on reset         90       I/O       USB.D_P       USB D+ Signal: high Z on reset         91       NC       Sector       Sector         93       O       I2CM.SCL       I2C Master Clock signal: connect I2C bus from LIM <th></th> <th></th> <th>PEN</th> <th>Module power enable</th>   |       |      | PEN         | Module power enable                                      |
| 76     0     SPI.SCLK     Not used - high Z       77     I/O     SPI.SIO0     Not used - high Z       78     I/O     SPI.SIO1     Not used - high Z       79     0     SPI.NCS     Not used - high Z       80     NC     NC       81     NC     Second - high Z       82     NC     Second - high Z       83     PWR     GND     Power ground       84     NC     Second - high Z       85     NC     Second - high Z       86     NC     Second - high Z       87     NC     Second - high Z       88     PWR     GND     Power ground       89     I/O     USB.D_N     USB D- Signal: high Z on reset       90     I/O     USB.D_P     USB D+ Signal: high Z on reset       91     NC     Second - S   |       | NC   |             |  |
| 77       I/O       SPI.SIO0       Not used - high Z         78       I/O       SPI.SIO1       Not used - high Z         79       O       SPI.nCS       Not used - high Z         80       NC       80       NC         81       NC       82       NC         83       PWR       GND       Power ground         84       NC       85       NC         85       NC       86       NC         86       NC       88       PWR       GND         89       I/O       USB.D_N       USB D- Signal: high Z on reset         90       I/O       USB.D_P       USB D+ Signal: high Z on reset         91       NC       92       NC         93       O       I2CM.SCL       I2C Master Clock signal: connect I2C bus from LIM         94       O       I2CM.SDA       I2C Master Data signal: connect I2C bus from LIM  |       |      | SPI SCI K   | Not used – high Z  |
| 78     I/O     SPI.SIO1     Not used – high Z       79     O     SPI.nCS     Not used – high Z       80     NC     Not     Second Parameter       81     NC     Second Parameter     Second Parameter       82     NC     Second Parameter     Second Parameter       83     PWR     GND     Power ground       84     NC     Second Parameter     Second Parameter       85     NC     Second Parameter     Second Parameter       86     NC     Second Parameter     Second Parameter       87     NC     Second Parameter     Second Parameter       88     PWR     GND     Power ground     Second Parameter       89     I/O     USB.D_N     USB D- Signal: high Z on reset     Second Parameter       90     I/O     USB.D_P     USB D+ Signal: high Z on reset     Second Parameter       91     NC     Second Parameter     Second Parameter     Second Parameter       93     O     I2CM.SCL     I2C Master Clock signal: connect I2C bus from LIM       94     O     I2CM.SDA     I2C Master Data signal: connect I2C bus from LIM  <   |       |      |             | -  |
| 79       O       SPI.nCS       Not used – high Z         80       NC          81       NC          82       NC          83       PWR       GND       Power ground         84       NC           85       NC           86       NC           87       NC           88       PWR       GND       Power ground         89       I/O       USB.D_N       USB D- Signal: high Z on reset         90       I/O       USB.D_P       USB D+ Signal: high Z on reset         91       NC           92       NC           93       O       I2CM.SCL       I2C Master Clock signal: connect I2C bus from LIM         94       O       I2CM.SDA       I2C Master Data signal: connect I2C bus from LIM  |       |      |             |  |
| 80     NC       81     NC       82     NC       83     PWR     GND     Power ground       84     NC       85     NC       86     NC       87     NC       88     PWR       6ND     Power ground       89     I/O     USB.D_N       90     I/O     USB.D_P       91     NC       92     NC       93     O     I2CM.SCL       94     O     I2CM.SDA   |       |      |             |  |
| 81NC82NC83PWRGNDPower ground84NC85NC86NC87NC88PWRGNDPower ground89I/OUSB.D_NUSB D- Signal: high Z on reset90I/OUSB.D_PUSB D+ Signal: high Z on reset91NC92NC93OI2CM.SCLI2C Master Clock signal: connect I2C bus from LIM94OI2CM.SDAI2C Master Data signal: connect I2C bus from LIM   |       |      |             | 5  |
| 82NC83PWRGNDPower ground84NC85NC86NC87NC88PWRGNDPower ground89I/OUSB.D_NUSB D- Signal: high Z on reset90I/OUSB.D_PUSB D+ Signal: high Z on reset91NC92NC93OI2CM.SCLI2C Master Clock signal: connect I2C bus from LIM94OI2CM.SDAI2C Master Data signal: connect I2C bus from LIM   |       |      |             |  |
| 83PWRGNDPower ground84NC85NC86NC87NC88PWRGNDPower ground89I/OUSB.D_NUSB D- Signal: high Z on reset90I/OUSB.D_PUSB D+ Signal: high Z on reset91NC92NC93OI2CM.SCLI2C Master Clock signal: connect I2C bus from LIM94OI2CM.SDAI2C Master Data signal: connect I2C bus from LIM   |       |      |             |  |
| 84NC85NC86NC87NC88PWRGNDPower ground89I/OUSB.D_NUSB D- Signal: high Z on reset90I/OUSB.D_PUSB D+ Signal: high Z on reset91NC92NC930I2CM.SCLI2C Master Clock signal: connect I2C bus from LIM940I2CM.SDAI2C Master Data signal: connect I2C bus from LIM   |       | PWR  | GND         | Power ground   |
| 86NC87NC88PWRGNDPower ground89I/OUSB.D_NUSB D- Signal: high Z on reset90I/OUSB.D_PUSB D+ Signal: high Z on reset91NC92NC930I2CM.SCLI2C Master Clock signal: connect I2C bus from LIM940I2CM.SDAI2C Master Data signal: connect I2C bus from LIM   |       | NC   |             |  |
| 87NC88PWRGNDPower ground89I/OUSB.D_NUSB D- Signal: high Z on reset90I/OUSB.D_PUSB D+ Signal: high Z on reset91NC92NC93OI2CM.SCLI2C Master Clock signal: connect I2C bus from LIM94OI2CM.SDAI2C Master Data signal: connect I2C bus from LIM   | 85    | NC   |             |  |
| 88PWRGNDPower ground89I/OUSB.D_NUSB D- Signal: high Z on reset90I/OUSB.D_PUSB D+ Signal: high Z on reset91NC92NC93OI2CM.SCLI2C Master Clock signal: connect I2C bus from LIM94OI2CM.SDAI2C Master Data signal: connect I2C bus from LIM   | 86    | NC   |             |  |
| 89I/OUSB.D_NUSB D- Signal: high Z on reset90I/OUSB.D_PUSB D+ Signal: high Z on reset91NC92NC93OI2CM.SCLI2C Master Clock signal: connect I2C bus from LIM94OI2CM.SDAI2C Master Data signal: connect I2C bus from LIM   | 87    |      |             |  |
| 90I/OUSB.D_PUSB D+ Signal: high Z on reset91NC92NC93OI2CM.SCLI2C Master Clock signal: connect I2C bus from LIM94OI2CM.SDAI2C Master Data signal: connect I2C bus from LIM   |       |      |             |  |
| 91     NC       92     NC       93     O     I2CM.SCL     I2C Master Clock signal: connect I2C bus from LIM       94     O     I2CM.SDA     I2C Master Data signal: connect I2C bus from LIM  |       |      |             |  |
| 92NC93OI2CM.SCLI2C Master Clock signal: connect I2C bus from LIM94OI2CM.SDAI2C Master Data signal: connect I2C bus from LIM   |       |      | USB.D_P     | USB D+ Signal: high Z on reset                           |
| 930I2CM.SCLI2C Master Clock signal: connect I2C bus from LIM940I2CM.SDAI2C Master Data signal: connect I2C bus from LIM   |       |      |             |  |
| 94 O I2CM.SDA I2C Master Data signal: connect I2C bus from LIM  |       |      |             |  |
| Ğ   |       |      |             |  |
| 95 PWR GND Power ground   |       |      |             | <u> </u>   |
|   | 95    | PWR  | GND         | Power ground   |

Template No.: 900-306 / A



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|-------|------|-------------|-----------------|-----------|
| Pin # | Туре | Signal name | Description     |           |
| 96    | PWR  | GND         | Power ground    |           |
| 97    | PWR  | VIN         | 5V Power supply |           |
| 98    | PWR  | VIN         | 5V Power supply |           |
| 99    | PWR  | VIN         | 5V Power supply |           |
| 100   | PWR  | VIN         | 5V Power supply |           |
| 101   | PWR  | GND         | Power ground    |           |
| 102   | PWR  | GND         | Power ground    |           |
| 103   | PWR  | GND         | Power ground    |           |
| 104   | PWR  | GND         | Power ground    |           |
| 105   | PWR  | GND         | Power ground    |           |
| 106   | PWR  | GND         | Power ground    |           |
| 107   | PWR  | GND         | Power ground    |           |
| 108   | PWR  | GND         | Power ground    |           |
| 109   | PWR  | GND         | Power ground    |           |
| 110   | PWR  | GND         | Power ground    |           |
|       |      |             |                 |           |

Table 1 Pin-out of the TIM<sup>uP</sup> – 19k-S3-Spartan6 connector

#### 3.1 Timing of Trigger Input Pin

When the module is set to hardware trigger mode, a rising edge on the trigger input pin causes the camera to force an immediate frame capture. The typical timing constraints are shown in Table 2 Hardware trigger timing



| Timing value    | Description                           | Min | Typical | Max | Unit |  |
|-----------------|---------------------------------------|-----|---------|-----|------|--|
| t <sub>PL</sub> | Pulse Low Time before Trigger         | 50  |         |     | ns   |  |
| teн             | Pulse High Time                       | 50  |         |     | ns   |  |
| <b>L</b> AT     | Trigger Edge to Frame Capture Latency | TBD | 60      | TBD | μs   |  |

Table 2 Hardware trigger timing

#### 3.2 Timing of Trigger Output Pin

The trigger output pin can be used for a synchronization of several TIM<sup>uP</sup>-19kS3-Spartan6 modules by connecting the trigger output pin of one module to the trigger input pin of the following module. The trigger output pin defaults to low and goes high for a short time right after the modulation phases.





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## 4 Interfacing

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The TIM<sup>uP</sup> - 19k-S3-Spartan6 firmware provides a USB data and control interface, an ISM parallel sensor interface and I<sup>2</sup>C control interface. All interfaces are exposed on the 100pin board to board connector.

The interfaces are split into a control and data interface. The control interface is used to set and read the configuration of the TIM<sup>uP</sup> - 19k-S3-Spartan6 module using a set of registers.

#### Note

For a complete register description refer to:

5 Register Description

#### 4.1 General Data Format

The data output format on both, the USB and the ISM interface, is divided into four containers where each container has its own header. The data containers hold the pixel information whereas the header consists of 128 32bit double words of data stored in high byte first order. By default, the first data container and its header are disabled. The three remaining data containers are configured as follows:

- Data container 0: disabled
- Data container 1: phase values [0..0xffff equal to a phase of 0..2π]
- Data container 2: amplitudes [0..0xffff]
- Data container 3: plausibility flags

| Header | Data Container 0 | Header | Data Container 1 | Header | Data Container 2 | Header | Data Container 3 |
|--------|------------------|--------|------------------|--------|------------------|--------|------------------|
|        |                  |        |                  |        |                  |        |                  |

Figure 4-1 Data Containers

#### Note

For a complete description of the header data refer to:

## 4.2 🏼 🏷 5.3 Change Modulation Frequency

The TIMuP-19k-S3-Spartan6 module has two PLLs where two modulation frequencies can be configured simultaneously. The switch between the two modulation frequencies can be performed without reconfiguration of the PLLs and so without a delay. This modulation frequencies are set to 10MHz and 20MHz in registers ModulationFrequency0 and ModulationFrequency1 by default.

When it comes to configure the Frame capture sequence, one of the two modulation frequencies can be selected using the SeqXPLLSelect register or by setting the appropriate frequency in SeqXModFreq register. Both methods lead to the same result. The modulation frequency used in any sequency can never be different to the configured frequencies in ModulationFrequency0 or ModulationFrequency1 register. The ModulationFrequency0 and ModulationFrequency1 register have to be set to the appropriate value before setting the sequences modulation frequency. Changing the registers ModulationFrequency0/1 registers will lead to a PLL setup phase of 200ms where a frame trigger is not possible.



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When changing the modulation frequency to one of the values predefined in the offset registers, the offset will also automatically be set in the appropriate SeqXOffset register. This value can be overridden by setting the SeqXOffset Register again to the desired value.

#### 4.3 Software trigger mode

In software trigger mode, the TIMuP-19k-S3-Spartan6 module is waiting in idle mode without capturing any frames until the register "SoftwareTrigger – 0x22" is set. Then one frame is triggered immediately and delivered in the ISM interface or provided on the USB. The typical delay until the frame is delivered is calculated as follows:

4 \* *IntegrationTime* + *fixme* 

#### 4.4 Multiple Sequences

At the moment, the TIMuP-19k-S3-Spartan6 module provides two sequences which can be configured independently. The number of triggered sequences can be configured in register "SequenceLength – 0x0B". When set to 2 every frame trigger will result in two frames. In freerun mode 40 frames per second will lead to 80 frames delivered on the ISM interface or provided on the USB. The two sequence frames are taken without a delay in between. Use cases of multiple sequences are for example:

- Multiple modulation frequencies to extend the ambiguity range
- Multiple integration times to extend the dynamic range

Header Description

#### Note

To calculate the distance you must multiply the phase value with  $\frac{c_{2f}}{0xfff}$ 

$$dist = (\text{phase value}) * \frac{c/2f}{65535}$$

dist... distance [m] c...speed of light  $[m/s^2]$ f...modulation frequency [Hz]

If the resulting value is greater than the ambiguity range subtract the ambiguity range. If the value is less than 0, add the ambiguity range.

This only applies to ISM data interface! In USB mode the SDK does all the calculation to get correct distances in mm.

#### 4.5 USB Interface

For interfacing the TIM<sup>uP</sup>-19k-S3-Spartan6 module over USB, a powerful SDK is provided. The SDK runs under Linux and Windows. Refer to our support website for downloading the SDK, sample code, for additional information and documentation.

#### Software and documentation

https://support.bluetechnix.at/wiki/TIM-UP-19k-S3-Spartan6



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#### 4.6 ISM / I<sup>2</sup>C Interface

#### 4.6.1 I<sup>2</sup>C Configuration Interface

The TIM<sup>uP</sup>-19k-S3-Spartan6 module can be configured using an I<sup>2</sup>C connection. The I<sup>2</sup>C control interface of the TIM<sup>uP</sup>-19k-S3-Spartan6 module is listening on the following I<sup>2</sup>C slave address:

- I<sup>2</sup>C Address: 0x5D
- SCL Frequency: up to 400kHz

The TIM<sup>uP</sup> - 19k-S3-Spartan6 module has a set of 32bit registers and is addressed by a 16bit address pointer. Following two figures show the timing diagrams of the I2C read and write.



Figure 4-2 I<sup>2</sup>C register read timing diagram



Figure 4-3 I<sup>2</sup>C register write timing diagram

#### Note

For a complete register description refer to:

b Register Description

#### 4.6.2 ISM Data Interface

When configured to stream data over ISM in free run mode, the TIM<sup>uP</sup> - 19k-S3-Spartan6 module starts transferring frames automatically and can only be interrupted by switching to manual trigger mode.

Each frame starts with a rising edge on the VSYNC signal followed by a rising edge of the HSYNC signal. With the first HSYNC signal, the first data block is transmitted as shown in Figure 4-4 Timing diagram of the ISM data interface. Every data block contains 512bytes and starts with a HSYNC.





Figure 4-4 Timing diagram of the ISM data interface

Data comes low byte first and has to be captured on every rising edge starting with the rising edge of the HSYNC signal.



Figure 4-5 Byte order of the ISM data interface

The data stream during one frame is continuous, there is no horizontal blanking before the next HSYNC. The vertical blanking period varies depending on frame rate. Once ISM.nDE is low, the pixel clock never stops. ISM.PCLK stays constant at 48MHz.



## 5 Register Description

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The TIM<sup>uP</sup>-19k-S3-Spartan6 module has a continuous register set of 256 32bit registers which can be configured via the SDK in USB mode or I<sup>2</sup>C in ISM mode.

#### 5.1 General Registers

| Addr<br>(hex) | Register Name              | Default<br>Value<br>(hex) | R/W | Description  |
|---------------|----------------------------|---------------------------|-----|--|
| 00            | Status <sup>3)</sup>       | 0                         | R   | Bit[0]: Calc FIFO overflow<br>Bit[1]: frame dropped<br>Bit[2]: Watchdog caused reset<br>Bit[3:7]: reserved<br>Bit[8]: 1 FPN verified<br>Bit[9]: 1 FPN verified<br>Bit[10]: 0 default register map loaded<br>1 stored register map loaded<br>Bit[11]: 1 mainboard temperature sensor found<br>Bit[12]: 1 LED board temperature sensor found |
| 01            | SerialNumber <sup>1)</sup> | -                         | R   | Bit[0:19]: Serial Number<br>Bit[20:31]: Device Type  |
| 02            | ReleaseDate                | -                         | R   | Release date, hex value interpreted as date<br>For example 0x01012014 means 01.01.2014   |
| 03            | FrameSize                  | 1C800                     | R   | Frame size in bytes  |
| 04            | NumRows                    | 78                        | R   | Number of vertical pixels delivered  |
| 05            | NumColumns                 | AO                        | R   | Number of horizontal pixels delivered  |
| 0B            | SequenceLength             | 1                         | R/W | Number of sequences to be calculated   |
| 10            | TempMainboard              | -                         | R   | Temperature of Mainboard in fixedpoint 9.4 [°C]  |
| 11            | TempIllumination           | -                         | R   | Temperature of Illumination in fixedpoint 9.4 [°C]   |
| 16            | ChipsizeColumns            | AO                        | R   | Horizontal count of pixels (sensor)  |
| 17            | ChipsizeRows               | 78                        | R   | Vertical count of pixels (sensor)  |
| 18            | TimestampIncrement         | 1312D                     | R/W | desired timestamp granularity timer value<br>default: 78125 / 78125000 = 1ms   |
| 19            | TriggerMode                | 0                         | R/W | Bit[0:1]: 0 free run mode<br>1 hardware trigger mode<br>2 software trigger mode  |
| 1B            | TempIlluminationGain1      | 0                         | R/W | Coefficient c3 for cubic temperature compensation of the illumination module temperature x/10000   |
| 1C            | TempIlluminationGain2      | 0                         | R/W | Coefficient c2 for cubic temperature compensation of the illumination module temperature x/10000   |
| 1D            | TempIlluminationGain3      | 0                         | R/W | Coefficient c1 for cubic temperature compensation of the illumination module temperature x/1000  |
| 1E            | TempMainboardGain1         | 0                         | R/W | Coefficient c3 for cubic temperature compensation of the mainboard temperature x/10000   |
| 1F            | TempMainboardGain2         | 0                         | R/W | Coefficient c2 for cubic temperature compensation of the mainboard temperature x/10000   |
| 20            | TempMainboardGain3         | 0                         | R/W | Coefficient c1 for cubic temperature compensation of the mainboard temperature x/1000  |



|               |                                 |                           |     | Version /   |
|---------------|---------------------------------|---------------------------|-----|---|
| Addr<br>(hex) | Register Name                   | Default<br>Value<br>(hex) | R/W | Description   |
| 21            | TempLimit                       | 46                        | R/W | Temperature limit for over temperature protection of<br>the illumination module (only available if TIM gets LED<br>board temperature!)                                    |
| 22            | SoftwareTrigger                 | 0                         | R/W | Set 1 to trigger a frame capture when in software trigger mode (Register 0x19)  |
| 30            | ModLedEnable <sup>2)</sup>      | 1B                        | R/W | Bit[0]: reserved - high<br>Bit[1]: enable differential LED mod signal<br>Bit[2]: enable single ended LED mod signal<br>Bit[3]: reserved - high<br>Bit[4]: reserved - high |
| 31            | StatusLedEnable <sup>2)</sup>   | 0                         | R/W | Bit[0]: 0 Status LED disabled<br>1 Status LED enabled   |
| 36            | AdvancedFunctions <sup>3)</sup> | 0                         | R/W | Bit[0:3]: 0 Watchdog disabled<br>1 Watchdog enabled<br>Bit[24:27]: 1 reset to factory default register set,<br>reboot required<br>Bit[28:31]: 1 reset module              |
| 37            | DataInterfaceType               | 0                         | R/W | Bit[0]: 0 USB data interface<br>1 ISM data interface  |
| 38            | FirmwareInfo                    | -                         | R   | Bit[0:5]: Firmware nonfunctional version<br>Bit[6:10]: Firmware minor version<br>Bit[11:15]: Firmware major version   |
| 76            | ModulationFrequency0            | 1312D00                   | R/W | First possible modulation frequency [Hz]  |
| 77            | ModulationFrequency1            | 989680                    | R/W | Second possible modulation frequency [Hz]   |
| 78            | 5MHz_Offset                     | 0                         | R/W | Offset for 5MHz modulation frequency [mm]   |
| 79            | 7.5MHz_Offset                   | 0                         | R/W | Offset for 7.5MHz modulation frequency [mm]   |
| 7A            | 10MHz_Offset                    | 0                         | R/W | Offset for 10MHz modulation frequency [mm]  |
| 7B            | 15MHz_Offset                    | 0                         | R/W | Offset for 15MHz modulation frequency [mm]  |
| 7C            | 20MHz_Offset                    | 0                         | R/W | Offset for 20MHz modulation frequency [mm]  |
| 7D            | 25MHz_Offset                    | 0                         | R/W | Offset for 25MHz modulation frequency [mm]  |
| 7E            | 30MHz_Offset                    | 0                         | R/W | Offset for 30MHz modulation frequency [mm]  |
| 7F            | FramesPerSecond                 | 5                         | R/W | FPS considering the configured sequence length and the corresponding integration times  |

Table 3 General registers description of the TIM<sup>uP</sup>-19k-S3-Spartan6

<sup>1)</sup> The Serial Number field contains the device type code and the serial number. For a list of all device type codes refer to:

https://support.bluetechnix.at/wiki/PMDSDK /\_PMDMDK\_User\_Manual#No.\_Serial.2FCustomer

<sup>2)</sup> For detailed information on hardware pins refer to:

3 Hardware Connector

<sup>3)</sup> Register available since Firmware v2.1.0



#### 5.2 Sequence Registers

| Addr<br>(hex) | Register Name                | Default<br>Value<br>(hex) | R/W | Description   |
|---------------|------------------------------|---------------------------|-----|---|
| 80            | Seq0PLLSelect                | 0                         | R/W | PLL config of the correct modulation frequency<br>Modulation frequency 0 and 1 are configured in register<br>76 and 77                |
| 81            | Seq0IntegrationTime          | 1F4                       | R/W | Integration time of sequence 0 in µs  |
| 82            | Seq0ModFreq                  | 1312D00                   | R/W | Modulation frequency to use for this sequence<br>Only modulation frequencies set in register 76 and 77<br>are valid for this register |
| 86            | Seq0DistOffset <sup>5)</sup> | 0                         | R/W | Override global offset  |
| 87            | Seq0AmpMin                   | 12C                       | R/W | Sets the minimal amplitude for valid pixels. Pixels with an amplitude below this value will be tagged by the amplitude low flag       |
| 8A            | Seq1PLLSelect                | 1                         | R/W | PLL config of the correct modulation frequency<br>Modulation frequency 0 and 1 are configured in register<br>76 and 77                |
| 8B            | Seq1IntegrationTime          | 1F4                       | R/W | Integration time of sequence 1 in µs  |
| 8C            | Seq1ModFreq                  | 989680                    | R/W | Modulation frequency to use for this sequence<br>Only modulation frequencies set in register 76 and 77<br>are valid for this register |
| 90            | Seq1DistOffset <sup>5)</sup> | 0                         | R/W | Override global offset  |
| 91            | Seq1AmpMin                   | 12C                       | R/W | Sets the minimal amplitude for valid pixels. Pixels with an amplitude below this value will be tagged by the amplitude low flag       |

Table 4 Sequence registers description of the TIM<sup>uP</sup> – 19k-S3-Spartan6

<sup>5)</sup> Distance offset is taken from global offset Registers 78 to 7E when SeqXPLLSelect or SeqXModFreq is set to one of the seven predefined Frequency values. This can be temporarily overridden to another offset.

#### 5.3 Change Modulation Frequency

The TIMuP-19k-S3-Spartan6 module has two PLLs where two modulation frequencies can be configured simultaneously. The switch between the two modulation frequencies can be performed without reconfiguration of the PLLs and so without a delay. This modulation frequencies are set to 10MHz and 20MHz in registers ModulationFrequency0 and ModulationFrequency1 by default.

When it comes to configure the Frame capture sequence, one of the two modulation frequencies can be selected using the SeqXPLLSelect register or by setting the appropriate frequency in SeqXModFreq register. Both methods lead to the same result.

The modulation frequency used in any sequency can never be different to the configured frequencies in ModulationFrequency0 or ModulationFrequency1 register. The ModulationFrequency0 and ModulationFrequency1 register have to be set to the appropriate value before setting the sequences modulation frequency. Changing the registers ModulationFrequency0/1 registers will lead to a PLL setup phase of 200ms where a frame trigger is not possible.

When changing the modulation frequency to one of the values predefined in the offset registers, the offset will also automatically be set in the appropriate SeqXOffset register. This value can be overridden by setting the SeqXOffset Register again to the desired value.



#### 5.4 Software trigger mode

Last change: 9 January 2015 Version 7

In software trigger mode, the TIMuP-19k-S3-Spartan6 module is waiting in idle mode without capturing any frames until the register "SoftwareTrigger – 0x22" is set. Then one frame is triggered immediately and delivered in the ISM interface or provided on the USB. The typical delay until the frame is delivered is calculated as follows:

4 \* IntegrationTime + fixme

#### 5.5 Multiple Sequences

At the moment, the TIMuP-19k-S3-Spartan6 module provides two sequences which can be configured independently. The number of triggered sequences can be configured in register "SequenceLength – 0x0B". When set to 2 every frame trigger will result in two frames. In freerun mode 40 frames per second will lead to 80 frames delivered on the ISM interface or provided on the USB. The two sequence frames are taken without a delay in between.

Use cases of multiple sequences are for example:

- Multiple modulation frequencies to extend the ambiguity range
- Multiple integration times to extend the dynamic range



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## 6 Header Description

The TIM<sup>uP</sup>-19k-S3-Spartan6 module delivers several useful registers in every frame header. The values in the header fields represent the register values during runtime when a new frame is delivered.

| Addr<br>(hex) | Header Field                 | Description  |
|---------------|------------------------------|--|
| 00            | Status                       | See register description                               |
| 01            | SerialNumber                 | See register description                               |
| 02            | ReleaseDate                  | See register description                               |
| 03            | FrameSize                    | See register description                               |
| 04            | NumRows                      | See register description                               |
| 05            | NumColumns                   | See register description                               |
| 0B            | SequenceLength               | See register description                               |
| 10            | TempMainboard                | See register description                               |
| 11            | TempIllumination             | See register description                               |
| 16            | ChipsizeColumns              | See register description                               |
| 17            | ChipsizeRows                 | See register description                               |
| 18            | TimestampIncrement           | See register description                               |
| 19            | TriggerMode                  | See register description                               |
| 60            | SeqPLLSelect                 | See register description                               |
| 61            | Seq0IntegrationTime          | See register description                               |
| 62            | Seq0ModFreq                  | See register description                               |
| 66            | Seq0DistOffset <sup>5)</sup> | See register description                               |
| 67            | Seq0AmpMin                   | See register description                               |
| 6A            | FrameCounter                 | Continuous numbered frame count                        |
| 6B            | TimeStamp                    | Timestamp of frame with granularity set in Register 18 |



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### 7 Support

#### 7.1 General Support

General support for products can be found at Bluetechnix' support site

#### Support Link

https://support.bluetechnix.at/wiki/TIM-UP-19k-S3-Spartan6

#### 7.2 Software Packages

Software packages and software downloads are for registered customers only

#### Support Link

https://support.bluetechnix.at/wiki/TIM-UP-19k-S3-Spartan6

#### 7.2.1 Related Products

• LIM-U-LED-850



#### 8 **Product History**

#### 8.1 Version Information

## 8.1.1 TIM<sup>uP</sup> – 19k-S3-Spartan6-USB

| 0x28042014 April 2014 | First preliminary version |
|-----------------------|---------------------------|

Table 5: Overview TIM<sup>uP</sup> – 19k-S3-Spartan6-USB firmware changes

#### 8.1.2 TIM<sup>uP</sup> – 19k-S3-Spartan6

| Version               | Release<br>date | Changes                     |
|-----------------------|-----------------|-----------------------------|
| 2.0.0<br>(0x19082014) | 2014 08 19      | See release notes of v2.0.0 |
| 2.1.0                 | TBD             |                             |

Table 6: Overview TIM<sup>uP</sup> – 19k-S3-Spartan6-ISM firmware changes

#### 8.2 Anomalies

| Version | Date       | Description   |
|---------|------------|---|
| v0.0.0  | 2014 04 28 | No anomalies reported yet.  |
| v2.0.0  | 2014 08 19 | Compatibility to PMDSDK v0.3.0:<br>To get correct distance values when setting a new modulation frequency, a<br>disconnect and reconnect has to be performed! |
| v2.0.0  | 2014 11 10 | Switching to ISM/I2C Interface when USB was connected fails. I2C connection will not be established   |

Table 7 – Product anomalies

#### 8.3 Document Revision History

| Version | Date       | Document Revision  |
|---------|------------|--|
| 1       | 2014 04 28 | First release V1.0 of the Document   |
| 2       | 2014 05 16 | Unused Pins changed from pulldown to high-Z                                    |
| 3       | 2014 08 01 | Description of phase values added  |
| 4       | 2014 08 07 | USB and ISM interfaces merged, register description updated                    |
| 5       | 2014 08 19 | Added new Modulation Frequency description and finalized SUM for v2.0.0 update |
| 6       | 2014 09 15 | FirmwareInfo register description modified                                     |
| 7       | 2014 11 24 | Updates related to firmware v2.1.0   |

Table 8: Revision history

Last change: 9 January 2015 Version 7



Last change: 9 January 2015 Version 7

## 9 List of Abbreviations

| Abbreviation     | Description                                 |  |  |
|------------------|---|--|--|
| CSI              | Camera Sensor Interface                     |  |  |
| DC               | Direct Current                              |  |  |
| EBI              | External Bus Interface                      |  |  |
| ESD              | Electrostatic Discharge                     |  |  |
| FPN              | Fixed Pattern Noise                         |  |  |
| FPPN             | Fixed Phase Pattern Noise                   |  |  |
| GPIO             | General Purpose Input Output                |  |  |
| I                | Input                                       |  |  |
| I <sup>2</sup> C | Inter-Integrated Circuit                    |  |  |
| I/O              | Input/Output                                |  |  |
| ISM              | Image Sensor Module                         |  |  |
| NC               | Not Connected                               |  |  |
| 0                | Output                                      |  |  |
| OS               | Operating System                            |  |  |
| PPI              | Parallel Peripheral Interface               |  |  |
| PWR              | Power                                       |  |  |
| ROI              | Region Of Interest                          |  |  |
| SPI              | Serial Peripheral Interface                 |  |  |
| SPORT            | Serial Port                                 |  |  |
| UART             | Universal Asynchronous Receiver Transmitter |  |  |
| USB              | Universal Serial Bus                        |  |  |

Table 9: List of abbreviations



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