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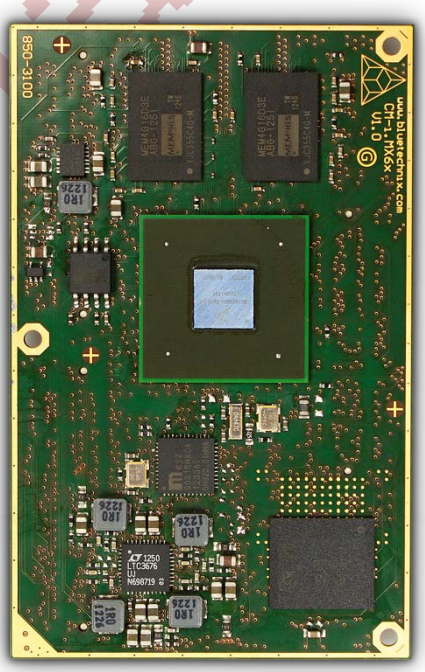
Embedding Ideas

CM-i.MX6x



Hardware User Manual

Version 1.1

Preliminary

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Warning

Due to technical requirements components may contain dangerous substances.

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1 Introduction

The SoM CM-i.MX6x is based on Freescale's next generation, high-performance, power-efficient, consumer multimedia applications processor family i.MX6. The SoM is available for both, commercial and industrial temperature range. It addresses 2 GByte of DDR3-SDRAM, has an onboard SPI NOR-flash of 2MByte and an eMMC-Flash of up to 4GByte.

The state of the art i.MX6 SoM in combination with the outstanding integration of several peripheral controllers, memory and voltage control, turn the CM-i.MX6x into a high-performance embedded platform for your future applications.

1.1 Overview

Figure 1-1 shows the main components of the CM-i.MX6x.

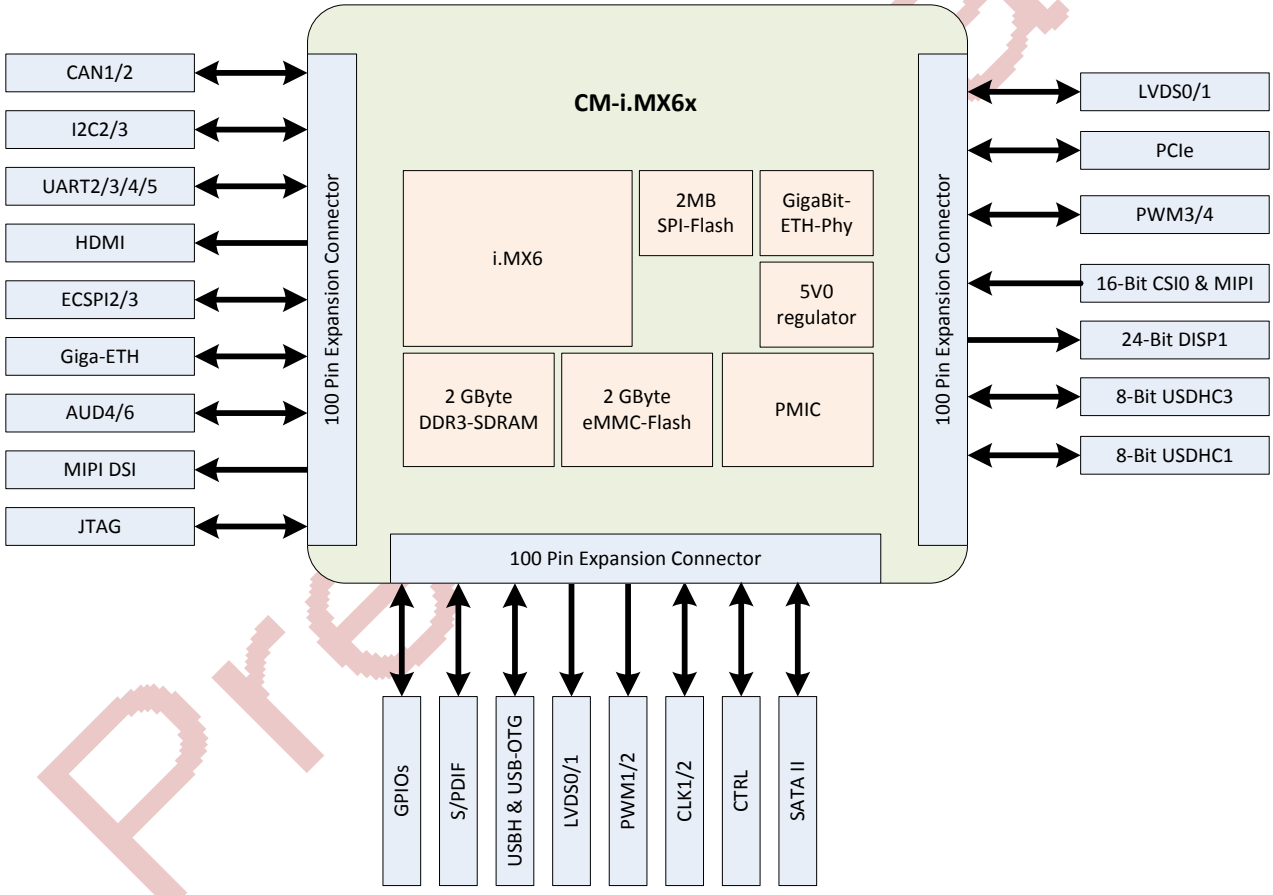

Figure 1-1: Main Components of the CM-i.MX6x

1.2 Key Features

- **Freescale Application Processor i.MX6**
  - Quad-Core – Industrial version
    - MCIMX6Q7CVT08AC

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  - Quad-Core – Commercial version
    - MCIMX6Q5EYM10AC
  - Dual-Core – Industrial version
    - MCIMX6D7CVT08AC
  - Dual-Core – Commercial version
    - MCIMX6D5EYM10AC

- **2 GByte DDR3-SDRAM**
  - Industrial version
    - TBD
    - DDR3-SDRAM Clock up to 533MHz
    - 4x (32Mbit x16 x 8 banks, 4Gbit at 1.35V)
  - Commercial version
    - TBD
    - DDR3-SDRAM Clock up to 533MHz
    - 4x (32Mbit x16 x 8 banks, 4Gbit at 1.35V)

- **2 GByte eMMC-Flash or MicroSD-card slot**
  - Industrial version
    - TBD
    - (16Gbit at 3.3V)
  - Commercial version
    - TBD
    - (16Gbit at 3.3V)

- **2 MByte SPI-Flash**
  - W25Q16BVSSIG
  - (16Mbit at 3.3V)

- **PMIC**
  - LTC3676EUJ#PBF & TPS63020DSJT
  - Energy Management
  - Power-up sequencer

- **Gigabit Ethernet PHY**
  - KSZ9031RNXCA

- **Interfaces**
  - 5x UART
  - 2x SPI
  - 2x I^2C
  - 2x CAN
  - 2x 8-Bit SDIO
  - 1x 24-Bit Parallel Display
  - 1x HDMI
  - 2x LVDS
  - 2x DSI-Lanes
  - 1x Gigabit Ethernet
  - 2x AUD
  - 1x S/PDIF
  - 1x 16-Bit CSI
  - 4x CSI-Lanes

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- 4x PWM
- 2x CLK
- 1x USBOTG
- 1x USBH
- 1x SATA II
- 1x PCIe
- GPIOs
- CTRL
- JTAG
- Power Supply

1.3 Applications

- Tablets
- Smart Mobile Devices
- Human-Machine-Interface
- 3D-Cameras
- Medical Devices
- Video Conference Systems
- Imaging and Consumer Multimedia
- Set Top Boxes
- Video Conference Applications
- Portable Media Players
- Industrial Applications

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2 General Description

2.1 Functional Description

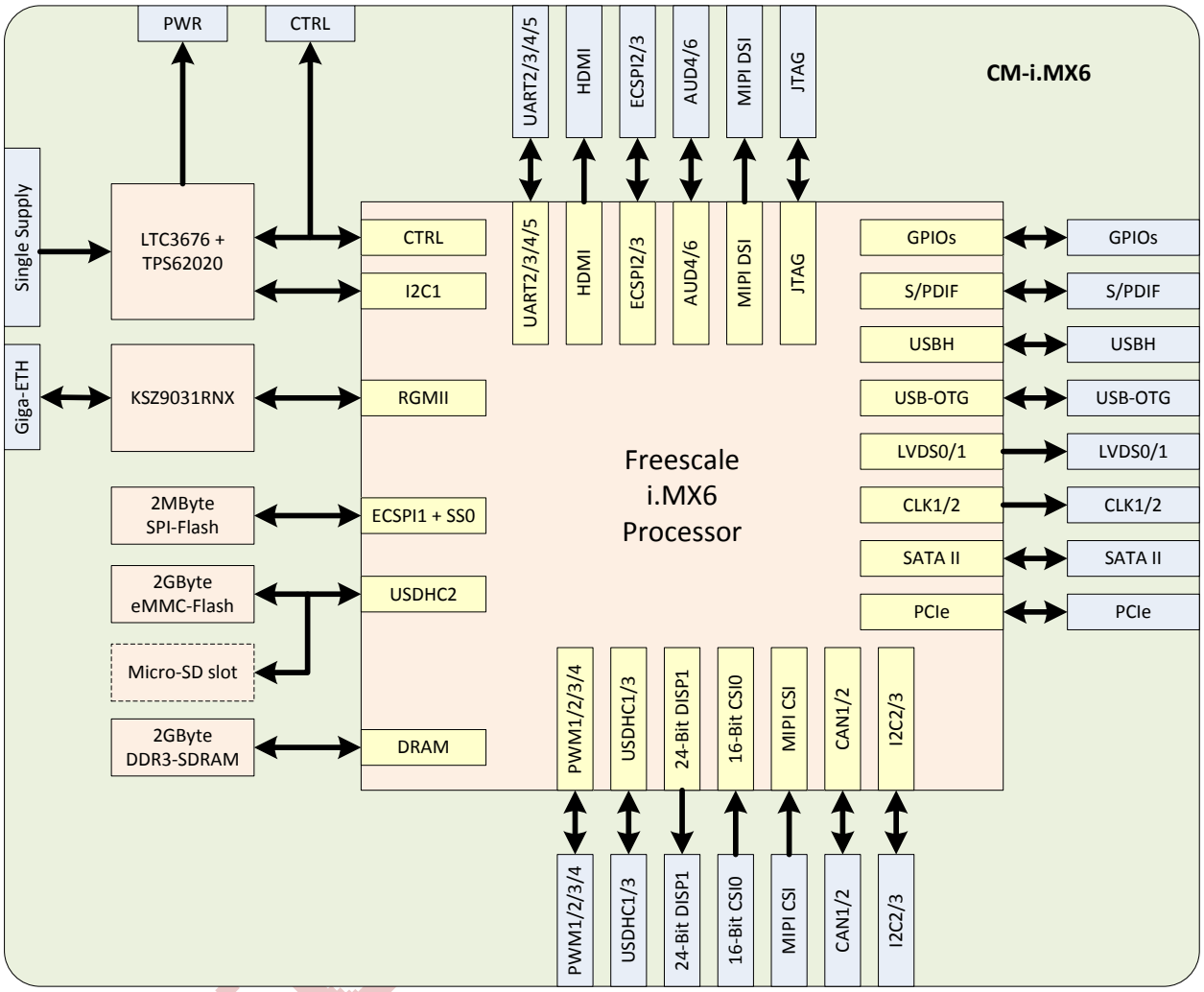

Figure 2-1 Detailed block diagram of the CM-i.MX6

2.1.1 PMIC

The power supplies for the i.MX6 processor are generated with the PMIC LTC3676 of Linear Technology in conjunction with the Buck-Boost-Converter TPS62020 of Texas Instruments. The PMIC can be configured through the I2C1 interface of the i.MX6.

2.1.2 Gigabit Ethernet

The CM-i.MX6x has the Gigabit Ethernet PHY KSZ9031RNX of Micrel onboard. The Gigabit Ethernet PHY is connected through RGMII with the i.MX6.

2.1.3 DDR3 SDRAM

The CM-i.MX6 provides 2 GByte of DDR3 SDRAM onboard.

2.1.4 eMMC Flash

The CM-i.MX6 provides 2 GByte of eMMC Flash onboard. The eMMC memory is connected through the USDHC2 interface with the i.MX6.

2.1.5 MicroSD-Support

An optional MicroSD-slot can be mounted on the bottom side of the CM-i.MX6. The MicroSD card shares the interface to the i.MX6 with the eMMC Flash (USDHC2). Both memories can be used simultaneously using the appropriate card identification mode (see Secure Digital Card Specification).

2.1.6 SPI Flash

The CM-i.MX6 provides 2 MByte of SPI Flash connected to the ECSPI1 and SS0 as chip select signal.

2.2 Boot Mode

The overall boot mode of the i.MX6 processor is determined by the BOOT_MODE[1:0] pins. For Internal Boot mode (BOOT_MODE[1:0] = 10), boot media is selected either by internal fuses, or by GPIOs which are sampled at power-up. For burning boot fuses, please consult the i.MX6 Reference Manual and the Software User Manual for the CM-i.MX6.

If boot media selection by GPIO sampling is desired, pull-down or pull-up resistors must be added to the specified pins. See chapter 4 for the voltage level of these pins. Consult the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (Freescale Document ID *IMX6DQ6SDLHDG*) for pull-down/-up recommendations.

Table 2-1 contains permitted configuration options of BOOT_MODE pins, where **0** means logic low and **1** means logic high. Consult aforementioned *Hardware Development Guide* for how to achieve these logic levels.

CM-i.MX6 Pin	Internal Boot (see below)	Serial Downloader (USB)	Boot From Fuses
BOOT_MODE0	0	1	0
BOOT_MODE1	1	0	0

Table 2-1: Boot mode pins

Table 2-2 contains the fuse/GPIO settings for the Internal Boot mode. An **empty cell** means that this pin's value is not considered for a specific boot setting. A cell marked with **X** means that the setting depends on your base board/custom boot flash. Please consult the *i.MX 6Dual/6Quad Applications Processor Reference Manual* (Freescale Doc. ID *IMX6DQRM*) to get more information.

CM-i.MX6 Pin	eFuse Name	SPI flash on SoM (ECSPI1)	External SPI flash (ECSPI3)	External SD/MMC (USDHC1)	eMMC on SoM (USDHC2)	External SD/MMC (USDHC3)	External SATA disk
DISP1.DAT9	BOOT_CFG10			**X**		**X**	
DISP1.DAT8	BOOT_CFG11			**0**	**0**	**X**	

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CM-i.MX6 Pin	eFuse Name	SPI flash on SoM (ECSPI1)	External SPI flash (ECSPI3)	External SD/MMC (USDHC1)	eMMC on SoM (USDHC2)	External SD/MMC (USDHC3)	External SATA disk
DISP1.DAT7	BOOT_CFG12			**X**		**X**	
DISP1.DAT6	BOOT_CFG13			**X**	TBD	**X**	
DISP1.DAT5	BOOT_CFG14	**1**	**1**	**X**	TBD	**X**	**0**
DISP1.DAT4	BOOT_CFG15	**1**	**1**	**X**	**1**	**X**	**1**
DISP1.DAT3	BOOT_CFG16	**0**	**0**	**1**	**1**	**1**	**0**
DISP1.DAT2	BOOT_CFG17	**0**	**0**	**0**	**0**	**0**	**0**
DISP1.DAT1	BOOT_CFG20			**0**	**0**	**0**	**X**
DISP1.DAT0	BOOT_CFG21			**0**	TBD	**X**	**X**
DISP1.PIN15	BOOT_CFG22			**X**	**0**	**X**	**X**
DISP1.PIN2	BOOT_CFG23			**0**	**1**	**0**	**X**
DISP1.PIN3	BOOT_CFG24			**0**	**0**	**1**	**X**
GPIO.3_13	BOOT_CFG25			**X**	TBD	**X**	
GPIO.3_14	BOOT_CFG26			**X**	TBD	**X**	
DISP1.PIN1	BOOT_CFG27			**X**	TBD	**X**	
DISP1.CLK	BOOT_CFG30						
DISP1.DAT12	BOOT_CFG31						
DISP1.DAT13	BOOT_CFG32			Default **0** (792MHz ARM clock)			
DISP1.DAT14	BOOT_CFG33						
DISP1.DAT15	BOOT_CFG34						
DISP1.DAT16	BOOT_CFG35						
DISP1.DAT17	BOOT_CFG36			Default **0** (ROM code enables MMU and L1 D-cache)			
DISP1.DAT18	BOOT_CFG37			Default **0** (ROM code enables L1 I-cache)			
DISP1.DAT19	BOOT_CFG40	**0**	**0**				
GPIO.5_0	BOOT_CFG41	**0**	**1**				
ECSPI2.SS1	BOOT_CFG42	**0**	**0**				
DISP1.DAT11	BOOT_CFG43	**1**	**X**				
DISP1.DAT10	BOOT_CFG44	**0**	**X**				
ECSPI2.SS0	BOOT_CFG45	**0**	**X**				
ECSPI1.SS0	BOOT_CFG46						
UART3.RTS	BOOT_CFG47			Default **0**			

Table 2-2: Boot configuration pins

2.3 Memory Map

Component	Memory area	Chip select
2 GiB DDR3-SDRAM	0x1000_0000 - 0x8FFF_FFFF	DRAM_CS0

Please consult the i.MX6 Reference Manual for the complete memory maps.

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3 Specifications

3.1 Electrical Specifications

3.1.1 Operating Conditions

Symbol	Parameter	Test	Min	Typ	Max	Unit
V_{IN}	Input supply voltage		2.7	-	5.5	V
I_{3V3}	Input supply current @ V_{IN}=3.3V		TBD	-	1800 (see AN4509)	mA
$V_{P\_3V0\_STBY}$				TBD		
$I_{P\_3V0\_STBY}$				TBD		
V_{OH}	High level output voltage		OVDD - 0.15	-		V
V_{OL}	Low level output voltage		-	-	0.15	V
V_{IH}	High level DC input voltage		0.7 x OVDD	-	OVDD	V
V_{IL}	Low level DC input voltage		0	-	0.3 x OVDD	V
I_{SIO}	IO sink current		-	-	7	mA
I_{IN}	Input current (no pull-up/down)	Vin=0V Vin=OVDD	-1	-	1	µA
I_{IN}	Input current (22 kΩ pull-up)	Vin=0V Vin=OVDD	-	-	212 1	µA
I_{IN}	Input current (47 kΩ pull-up)	Vin=0V Vin=OVDD	-	-	100 1	µA
I_{IN}	Input current (100 kΩ pull-up)	Vin=0V Vin=OVDD	-	-	48 1	µA
I_{IN}	Input current (100 kΩ pull-down)	Vin=0V Vin=OVDD	-		1 48	µA
$I_{DEEPSLEEP}$	V_{IN} current in deep sleep mode		TBD	TBD	TBD	mA
I_{SLEEP}	V_{IN} current in sleep mode		TBD	TBD	TBD	mA
I_{IDLE}	V_{IN} current in deep sleep mode		TBD	TBD	TBD	mA
I_{TYP}	V_{IN} current in with core running at 400 MHz		TBD	TBD	TBD	mA
$I_{HIBERNATE}$	V_{IN} current in hibernate state		TBD	TBD	TBD	mA
I_{RTC}	V_{RTC} current		TBD	TBD	TBD	µA
f_{CCLKC}	Core clock frequency for commercial grade modules		-	-	1000	MHz
f_{CCLKDI}	Core clock frequency for Dual-Core industrial grade modules		-	-	850	MHz
f_{CCLKQI}	Core clock frequency for Quad-Core industrial grade modules		-	-	800	MHz

Table 3-1: Electrical characteristics

3.1.2 Maximum Ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only. Operation of the device at these or any other conditions greater than those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
V_{IO}	Input or output voltage	-0.5	OVDD+0.3	V

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Symbol	Parameter	Min	Max	Unit
V_{IN}	Input supply voltage	-0.3	6	V
I_{OH} / I_{OL}	Current per pin	0	7	mA
T_{AMBC}	Ambient temperature for consumer grade	0	70*	°C
T_{AMBI}	Ambient temperature for industrial grade	-40	105*	°C
T_{STO}	Storage temperature	-40	150	°C
T_{SLD}	Solder temperature for 10 seconds		260	°C
φ_{AMB}	Relative ambient humidity		90	%

Table 3-2: Absolute maximum ratings

* If extreme high ambient temperatures are expected (75°C in industrial environments or 60°C for commercial products), the user has to apply a heat dissipator on CPU and DDR-RAM (avoid heat accumulation!). In addition the die temperature should be monitored regularly, so that the CPU and RAM clock can be throttled if necessary.

3.1.3 Power Outputs

The CM-i.MX6x provides voltage references for the power domains used by the i.MX6. This power outputs are intended as voltage references.

Symbol	Description	U [V]	I_{max} [mA]
Vref_diff	Reference voltage for differential signals and others	2.5	10
Vref_3V3	Reference voltage for 3V3	3.3	200
Vref_5V0	Reference voltage for 5V0	5.0	250
Vref_2V5	Reference voltage for 2V5	2.5	120
Vref_CTRL	Reference voltage for control signals	3.0	10

Table 3-3: Power Outputs

3.1.4 ESD Sensitivity

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

3.1.5 Cooling

If the SoM is subject to high performance applications a cooling system should be planned to prevent damage to and guarantee the full functionality of the SoM. The requirement of a cooling system depends also from the ambient temperature.

The following test was performed in a conditioning cabinet:

Firmware

TBD

Results

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TBD

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4 Connector Description

For a detail signal description please consult the i.MX6 reference manual, available on the Freescale web site.

4.1 Connector X1

Pin No.	Signal Name	i.MX6 Ball Name	Type	Voltage Level	Function	Boot
1	ECSPI2.MISO	EIM_OE	I	Vref_3V3	SPI MISO / GPIO2_25	
2	ECSPI2.MOSI	EIM_CS1	O	Vref_3V3	SPI MOSI / GPIO2_24	
3	ECSPI2.SCLK	EIM_CS0	O	Vref_3V3	SPI Clock / GPIO2_23	
4	ECSPI2.SS0	EIM_RW	O	Vref_3V3	SPI Select0 / GPIO2_26	BOOT_CFG45
5	ECSPI2.SS1	EIM_LBA	O	Vref_3V3	SPI Select1 / GPIO2_27	BOOT_CFG42
6	Vref_3V3		PWR	3V3	3.3V Voltage Reference	
7	ECSPI3.MISO	DISP0_DAT2	I	Vref_3V3	SPI MISO / GPIO4_23	
8	ECSPI3.MOSI	DISP0_DAT1	O	Vref_3V3	SPI MOSI / GPIO4_22	
9	ECSPI3.SCLK	DISP0_DAT0	O	Vref_3V3	SPI CLK / GPIO4_21	
10	ECSPI3.SS0	DISP0_DAT3	O	Vref_3V3	SPI Select0 / GPIO4_24	
11	ECSPI3.SS1	DISP0_DAT4	O	Vref_3V3	SPI Select1 / GPIO4_25	
12	Vref_3V3		PWR	3V3	3.3V Voltage Reference	
13	SD1.CMD	SD1_CMD	O	Vref_3V3	SD Command / GPIO1_18	
14	SD1.CLK	SD1_CLK	O	Vref_3V3	SD Clock / GPIO1_20	
15	SD1.DAT0	SD1_DAT0	I/O	Vref_3V3	SD Data0 / GPIO1_16	
16	SD1.DAT1	SD1_DAT1	I/O	Vref_3V3	SD Data1 / GPIO1_17	
17	SD1.DAT2	SD1_DAT2	I/O	Vref_3V3	SD Data2 / GPIO1_19	
18	SD1.DAT3	SD1_DAT3	I/O	Vref_3V3	SD Data3 / GPIO1_21	
19	SD1.CD	gpio1_1	I	Vref_3V3	SD Card Detect / GPIO1_1	
20	GPIO3_14	EIM_DA14	I/O	Vref_3V3	GPIO3_14	BOOT_CFG26
21	GND		PWR	GND		
22	UART3.RTS	EIM_EB3	O	Vref_3V3	UART Request To Send / GPIO2_31	
23	UART3.CTS	EIM_D23	I	Vref_3V3	UART Clear To Send / GPIO3_23	BOOT_CFG47
24	UART3.TX	EIM_D24	O	Vref_3V3	UART Transmit Data / GPIO3_24	
25	UART3.RX	EIM_D25	I	Vref_3V3	UART Receive Data / GPIO3_25	
26	Vref_3V3		PWR	3V3	3.3V Voltage Reference	
27	UART2.CTS	SD4_DAT6	I	Vref_3V3	UART Clear To Send / GPIO2_13	
28	UART2.RTS	SD4_DAT5	O	Vref_3V3	UART Request To Send / GPIO2_14	
29	UART2.TX	SD4_DAT7	O	Vref_3V3	UART Transmit Data / GPIO1_7	
30	UART2.RX	SD4_DAT4	I	Vref_3V3	UART Receive Data / GPIO1_8	
31	GND		PWR	GND		
32	DISP1.PIN1	EIM_DA15	O	Vref_3V3	DISP1 Pin15 / GPIO3_10	BOOT_CFG27
33	Vref_3V3		PWR	3V3	3.3V Voltage Reference	

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Pin No.	Signal Name	i.MX6 Ball Name	Type	Voltage Level	Function	Boot
34	AUD4.RXC	DISP0_DAT19	I	Vref_3V3	AUD Receive Clock / GPIO5_13	
35	AUD4.RXFS	DISP0_DAT18	I	Vref_3V3	AUD Receive Frame Sync / GPIO5_12	
36	AUD4.RXD	DISP0_DAT23	I	Vref_3V3	AUD Receive Data / GPIO5_17	
37	AUD4.TXC	DISP0_DAT20	O	Vref_3V3	AUD Transmit Clock / GPIO5_14	
38	AUD4.TXD	DISP0_DAT21	O	Vref_3V3	AUD Transmit Data / GPIO1_13	
39	AUD4.TXFS	DISP0_DAT22	O	Vref_3V3	AUD Transmit Frame Sync / GPIO5_16	
40	Vref_3V3		PWR	3V3	3.3V Voltage Reference	
41	I2C2.SCL	KEY_COL3	O	Vref_3V3	I2C Clock / GPIO4_12	
42	I2C2.SDA	KEY_ROW3	I/O	Vref_3V3	I2C Data / GPIO4_13	
43	I2C3.SCL	gpio1_5	O	Vref_3V3	I2C Clock / GPIO1_5	
44	I2C3.SDA	gpio1_6	I/O	Vref_3V3	I2C Data / GPIO1_6	
45	Vref_3V3		PWR	3V3	3.3V Voltage Reference	
46	JTAG.TCK	JTAG_TCK	I	Vref_3V3	JTAG Test Clock	
47	JTAG.TMS	JTAG_TMS	I	Vref_3V3	JTAG Test Mode Select	
48	JTAG.TDI	JTAG_TDI	I	Vref_3V3	JTAG Test Data Input	
49	JTAG.TDO	JTAG_TDO	O	Vref_3V3	JTAG Test Data Output	
50	JTAG.TRSTB	JTAG_TRSTB	I	Vref_3V3	JTAG Test Reset	
51	GPIO.5_0	EIM_WAIT	I/O	Vref_3V3	EIM WAIT / GPIO5_0	
52	JTAG.MOD	JTAG_MOD	I	Vref_3V3	JTAG Mode Selection	
53	ETH.LED_ACT		O	Vref_3V3	ETH Activity LED Driver	
54	ETH.LED_SPD		O	Vref_3V3	ETH Speed LED Driver	
55	NC				Not Connected	
56	ETH.TXRX_A_N		I/O	3V3	ETH Data A-	
57	ETH.TXRX_A_P		I/O	3V3	ETH Data A+	
58	GND		PWR	GND		
59	ETH.TXRX_B_N		I/O	3V3	ETH Data B-	
60	ETH.TXRX_B_P		I/O	3V3	ETH Data B+	
61	GND		PWR	GND		
62	CAN1.TX	KEY_COL2	O	Vref_3V3	CAN Transmit Data / GPIO4_10	
63	CAN1.RX	KEY_ROW2	I	Vref_3V3	CAN Receive Data / GPIO4_11	
64	Vref_3V3		PWR	3V3	3.3V Voltage Reference	
65	UART4.RX	KEY_ROW0	I	Vref_3V3	UART Receive Data / GPIO4_7	
66	UART4.TX	KEY_COL0	O	Vref_3V3	UART Transmit Data / GPIO4_6	
67	GND		PWR	GND	Power Ground	
68	VIN		PWR	VIN	Power Supply	
69	VIN		PWR	VIN	Power Supply	
70	VIN		PWR	VIN	Power Supply	
71	VIN		PWR	VIN	Power Supply	
72	VIN		PWR	VIN	Power Supply	
73	GND		PWR	GND	Power Ground	
74	ETH.TXRX_C_N		I/O		ETH Data C-	

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Pin No.	Signal Name	i.MX6 Ball Name	Type	Voltage Level	Function	Boot
75	ETH.TXRX_C_P		I/O		ETH Data C+	
76	GND		PWR	GND		
77	ETH.TXRX_D_N		I/O	3V3	ETH Data D-	
78	ETH.TXRX_D_P		I/O	3V3	ETH Data D+	
79	Vref_diff		PWR	2V5	2.5V Voltage Reference	
80	HDMI.CLK_N	HDMI_CLKM	O	Vref_diff	HDMI Clock-	
81	HDMI.CLK_P	HDMI_CLKP	O	Vref_diff	HDMI Clock+	
82	HDMI.D0_N	HDMI_D0M	O	Vref_diff	HDMI Data0-	
83	HDMI.D0_P	HDMI_D0P	O	Vref_diff	HDMI Data0+	
84	HDMI.D1_N	HDMI_D1M	O	Vref_diff	HDMI Data1-	
85	HDMI.D1_P	HDMI_D1P	O	Vref_diff	HDMI Data1+	
86	HDMI.D2_N	HDMI_D2M	O	Vref_diff	HDMI Data2-	
87	HDMI.D2_P	HDMI_D2P	O	Vref_diff	HDMI Data2+	
88	SD1.DAT4	NANDF_D0	I/O	Vref_3V3	SD Data3 / GPIO2_0	
89	SD1.DAT5	NANDF_D1	I/O	Vref_3V3	SD Data3 / GPIO2_1	
90	SD1.DAT6	NANDF_D2	I/O	Vref_3V3	SD Data3 / GPIO2_2	
91	SD1.DAT7	NANDF_D3	I/O	Vref_3V3	SD Data3 / GPIO2_3	
92	GND		PWR	GND		
93	P_3V0_STBY		PWR	3V0	Standby power supply	
94	DSI.CLK_N	DSI_CLK0M	O	Vref_diff	DSI Clock-	
95	DSI.CLK_P	DSI_CLK0P	O	Vref_diff	DSI Clock+	
96	DSI.D0_N	DSI_D0M	O	Vref_diff	DSI Data0-	
97	DSI.D0_P	DSI_D0P	O	Vref_diff	DSI Data0+	
98	DSI.D1_N	DSI_D1M	O	Vref_diff	DSI Data1-	
99	DSI.D1_P	DSI_D1P	O	Vref_diff	DSI Data1+	
100	Vref_diff		PWR	2V5	2.5V Voltage Reference	

Table 4-1: Connector description X1

4.2 Connector X2

Pin No.	Signal Name	i.MX Ball Name	Type	Voltage Level	Function	Boot
101	SATA.TX_N	SATA_TXM	O	Vref_diff	SATA Transmit Data-	
102	SATA.TX_P	SATA_TXP	O	Vref_diff	SATA Transmit Data+	
103	GPIO.5_6	DISP0_DAT12	I/O	Vref_3V3	GPIO5_6	
104	GPIO.5_7	DISP0_DAT13	I/O	Vref_3V3	GPIO5_7	
105	GPIO.6_7	NANDF_CLE	I/O	Vref_3V3	Clock 2 output -	
106	GPIO.6_8	NANDF_ALE	I/O	Vref_3V3	Clock 2 output +	
107	Vref_diff		PWR	2V5	2.5V Voltage Reference	
108	USB_H.VBUS		PWR	Vref_5V0	USB VBUS	
109	USB_H.OC	gpio1_3	I	Vref_3V3	USB Over Current / GPIO1_3	
110	USB_H.PWR	gpio1_0	O	Vref_3V3	USB Power Enable / GPIO1_0	
111	GPIO.5_0	EIM_WAIT	I/O	Vref_3V3	GPIO5_0	BOOT_CFG41
112	USB_OTG.PWR	EIM_D22	O	Vref_3V3	USB Power Enable / GPIO3_22	
113	USB_OTG.ID	ENET_RX_ER	I	Vref_3V3	USB ID / GPIO1_24	

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Pin No.	Signal Name	i.MX Ball Name	Type	Voltage Level	Function	Boot
114	GND		PWR	GND		
115	SPDIF.SRCLK	gpio1_8	I	Vref_3V3	SPDIF SRCLK / GPIO1_8	
116	SPDIF.EXTCLK	ENET_CRS_DV	I	Vref_diff	SPDIF EXTCLK / GPIO1_25	
117	GND		PWR	GND		
118	SPDIF.IN	GPIO_16	I	Vref_3V3	SPDIF Input / GPIO7_11	
119	SPDIF.PLOCK	gpio1_7	O	Vref_3V3	SPDIF PLOCK / GPIO1_7	
120	GND		PWR	GND		
121	SPDIF.OUT	GPIO_17	O	Vref_3V3	SPDIF Output / GPIO7_12	
122	Vref_2V5		PWR	2V5	2.5V Voltage Reference (LDO)	
123	GPIO.6_31	EIM_BCLK	I/O	Vref_3V3	GPIO6_31	
124	GND		PWR	GND	AUDIO Headphone GND	
125	EPIT_OUT2	EIM_D20	O	Vref_3V3	EPIT2 Output / GPIO3_20	
126	PWM_OUT1	DISP0_DAT8	O	Vref_3V3	Pulse Width Modulation Output / GPIO4_29	
127	PWM_OUT2	DISP0_DAT9	O	Vref_3V3	Pulse Width Modulation Output / GPIO4_30	
128	GPIO.5_10	DISP0_DAT16	I/O	Vref_3V3	GPIO5_10	
129	CTRL.PWR_ON	EIM_D29	I			
130	Vref_CTRL		PWR	3V0	Voltage Reference for Control Signals	
131	CTRL.nRESET_IN		I		External Reset Input (Short to GND for Reset)	
132	CTRL.TAMPER	TAMPER	I		Tamper	
133	CTRL.nON		O		Start-Up PMIC if PIN is low for 400ms	
134	PMIC_STBY_REQ	PMIC_STBY_REQ	O			
135	WDOG1_B	GPIO1_9	I	Vref_3V3	Watchdog 1 / GPIO1_9	
136	GPIO.4_5	GPIO_19	I/O	Vref_3V3		
137	GND		PWR	GND		
138	CAN2.RX	KEY_ROW4	I	Vref_3V3	CAN RX / GPIO4_15	
139	CAN2.TX	KEY_COL4	O	Vref_3V3	CAN TX / GPIO4_14	
140	PWM_OUT3	SD4_DAT1	O	Vref_3V3	Pulse Width Modulation / GPIO2_9	
141	PWM_OUT4	SD4_DAT2	O	Vref_3V3	Pulse Width Modulation / GPIO2_10	
142	Vref_3V3		PWR	3V3	3.3V Voltage Reference	
143	EPIT_OUT1	EIM_D19	O	Vref_3V3	EPIT1 Output / GPIO3_19	
144	AUD6.RXC	DISP0_DAT6	I	Vref_3V3	AUD Receive Clock / GPIO4_27	
145	AUD6.RXFS	DISP0_DAT5	I	Vref_3V3	AUD Receive Frame Sync / GPIO4_26	
146	AUD6.RXD	DI0_PIN4	I	Vref_3V3	AUD Receive Data / GPIO4_20	
147	AUD6.TXC	DI0_PIN15	O	Vref_3V3	AUD Transmit Clock / GPIO4_17	
148	AUD6.TXD	DI0_PIN2	O	Vref_3V3	AUD Transmit Data / GPIO4_18	
149	AUD6.TXFS	DI0_PIN3	O	Vref_3V3	AUD Transmit Frame Sync / GPIO4_19	
150	GND		PWR	GND		
151	GND		PWR	GND		
152	ECSPI1.SS1	DISP0_DAT15	I/O	Vref_3V3	ECSPI1_SS1 / GPIO5_9	
153	GPIO.2_8	SD4_DAT0	I/O	Vref_3V3	GPIO2_8	
154	GPIO.7_10	SD4_CLK	I/O	Vref_3V3	GPIO7_10	
155	GPIO.5_11	DISP0_DAT17	I/O	Vref_3V3	GPIO5_11	
156	GPIO.3_13	EIM_DA13	I/O	Vref_3V3	GPIO3_13	BOOT_CFG25

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Pin No.	Signal Name	i.MX Ball Name	Type	Voltage Level	Function	Boot
157	Vref_3V3		PWR	3V3	3.3V Voltage Reference	
158	GND		PWR	GND		
159	GPIO.5_5	DISP0_DAT11	I/O	Vref_3V3	GPIO5_5	
160	GPIO.4_31	DISP0_DAT10	I/O	Vref_3V3	GPIO4_31	
161	GPIO.4_28	DISP0_DAT7	I/O	Vref_3V3	GPIO4_28	
162	GPIO.4_16	DI0_DISP_CLK	I/O	Vref_3V3	GPIO4_16	
163	Vref_diff		PWR	2V5	2.5V Voltage Reference	
164	CTRL.BM1	BOOT_MODE1	I	Vref_3V3	Boot Mode1	
165	CTRL.BM0	BOOT_MODE0	I	Vref_3V3	Boot Mode0	
166	VIN		PWR	VIN	Power Supply	
167	VIN		PWR	VIN	Power Supply	
168	VIN		PWR	VIN	Power Supply	
169	VIN		PWR	VIN	Power Supply	
170	GND		PWR	GND	Power Ground	
171	GND		PWR	GND	Power Ground	
172	GND		PWR	GND	Power Ground	
173	GND		PWR	GND	Power Ground	
174	SD3.VSELECT	GPIO_18	O	Vref_3V3	SDIO VSELECT / GPIO7_13	
175	SD3.RST	SD3_RST	O	Vref_3V3	SDIO Reset / GPIO7_8	
176	SD3.DAT7	SD3_DAT7	I/O	Vref_3V3	SDIO Data7 / GPIO6_17	
177	SD3.DAT6	SD3_DAT6	I/O	Vref_3V3	SDIO Data6 / GPIO6_18	
178	SD3.DAT5	SD3_DAT5	I/O	Vref_3V3	SDIO Data5 / GPIO7_0	
179	SD3.DAT4	SD3_DAT4	I/O	Vref_3V3	SDIO Data4 / GPIO7_1	
180	Vref_3V3		PWR	3V3	3.3V Voltage Reference	
181	SD3.DAT3	SD3_DAT3	I/O	Vref_3V3	SDIO Data3 / GPIO7_7	
182	SD3.DAT2	SD3_DAT2	I/O	Vref_3V3	SDIO Data2 / GPIO7_6	
183	SD3.DAT1	SD3_DAT1	I/O	Vref_3V3	SDIO Data1 / GPIO7_5	
184	SD3.DAT0	SD3_DAT0	I/O	Vref_3V3	SDIO Data0 / GPIO7_4	
185	SD3.CLK	SD3_CLK	O	Vref_3V3	SDIO CLK / GPIO7_3	
186	SD3.CMD	SD3_CMD	O	Vref_3V3	SDIO Command / GPIO7_2	
187	GND		PWR	GND		
188	USB_OTG.VBUS		PWR	Vref_5V0	USB VBUS	
189	USB_OTG.D_P	USB_OTG_DP	I/O	3V0	USB OTP Data+	
190	USB_OTG.D_N	USB_OTG_DN	I/O	3V0	USB OTP Data-	
191	GND		PWR	GND		
192	USB_H.D_P	USB_H1_DP	I/O	3V0	USB Data+	
193	USB_H.D_N	USB_H1_DN	I/O	3V0	USB Data-	
194	Vref_5V0		PWR	5V0	USB Voltage Reference	
195	GPIO.6_9	NANDF_WP_B	I/O	Vref_3V3	GPIO6_9	
196	CLK2.CLK_P	CLK2_P	I/O	Vref_diff	GPIO6_8	
197	CLK2.CLK_N	CLK2_N	I/O	Vref_diff	GPIO6_7	
198	GND		PWR	GND		
199	SATA.RX_P	SATA_RXP	I	Vref_diff	SATA Receive Data+	
200	SATA.RX_N	SATA_RXM	I	Vref_diff	SATA Receive Data-	

Table 4-2: Connector description X2

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4.3 Connector X3

Pin No.	Signal Name	i.MX Ball Name	Type	Voltage Level	Function	Boot
201	Vref_diff		PWR	2V5	2.5V Voltage Reference	
202	DISP1.D14	EIM_A19	O	Vref_3V3	DISP Data14 / GPIO2_19	BOOT_CFG33
203	DISP1.D15	EIM_A20	O	Vref_3V3	DISP Data15 / GPIO2_18	BOOT_CFG34
204	DISP1.D16	EIM_A21	O	Vref_3V3	DISP Data16 / GPIO2_17	BOOT_CFG35
205	DISP1.D17	EIM_A22	O	Vref_3V3	DISP Data17 / GPIO2_16	BOOT_CFG36
206	DISP1.D18	EIM_A23	O	Vref_3V3	DISP Data18 / GPIO6_6	BOOT_CFG37
207	DISP1.D19	EIM_A24	O	Vref_3V3	DISP Data19 / GPIO5_4	BOOT_CFG40
208	DISP1.D20	EIM_D31	O	Vref_3V3	DISP Data20 / GPIO3_31	
209	DISP1.D21	EIM_D30	O	Vref_3V3	DISP Data21 / GPIO3_30	
210	DISP1.D22	EIM_D26	O	Vref_3V3	DISP Data22 / GPIO3_26	
211	DISP1.D23	EIM_D27	O	Vref_3V3	DISP Data23 / GPIO3_27	
212	DISP1.CLK	EIM_A16	O	Vref_3V3	DISP Clock / GPIO2_22	BOOT_CFG30
213	DISP1.PIN2	EIM_DA11	O	Vref_3V3	DISP Pin1 / GPIO3_15	BOOT_CFG23
214	DISP1.PIN3	EIM_DA12	O	Vref_3V3	DISP Pin2/ GPIO3_11	BOOT_CFG24
215	DISP1.PIN15	EIM_DA10	O	Vref_3V3	DISP Pin3/ GPIO3_12	BOOT_CFG22
216	CSI.D0_P	CSI_D0P	I	Vref_diff	MIPI CSI Lane0+	
217	CSI.D0_N	CSI_D0M	I	Vref_diff	MIPI CSI Lane0-	
218	CSI.D1_P	CSI_D1P	I	Vref_diff	MIPI CSI Lane1+	
219	CSI.D1_N	CSI_D1M	I	Vref_diff	MIPI CSI Lane1-	
220	CSI.D2_P	CSI_D2P	I	Vref_diff	MIPI CSI Lane2+	
221	CSI.D2_N	CSI_D2M	I	Vref_diff	MIPI CSI Lane2-	
222	CSI.D3_P	CSI_D3P	I	Vref_diff	MIPI CSI Lane3+	
223	CSI.D3_N	CSI_D3M	I	Vref_diff	MIPI CSI Lane3-	
224	CSI.CLK_P	CSI_CLK0P	O	Vref_diff	MIPI CSI Clock+	
225	CSI.CLK_N	CSI_CLK0M	O	Vref_diff	MIPI CSI Clock-	
226	GND		PWR	GND	Signal Ground	
227	UART5.TX	KEY_COL1	O	Vref_3V3	UART5 RX / GPIO4_9	
228	UART5.RX	KEY_ROW1	I	Vref_3V3	UART5 TX / GPIO4_8	
229	GND		PWR	GND	Signal Ground	
230	CSI0.D9	CSI0_D9	I	Vref_3V3	CSI Data9 / GPIO5_27	
231	CSI0.D8	CSI0_D8	I	Vref_3V3	CSI Data8 / GPIO5_26	
232	CSI0.D7	CSI0_D7	I	Vref_3V3	CSI Data7 / GPIO5_25	
233	CSI0.D6	CSI0_D6	I	Vref_3V3	CSI Data6 / GPIO5_24	
234	CSI0.D5	CSI0_D5	I	Vref_3V3	CSI Data5 / GPIO5_23	
235	CSI0.D4	CSI0_D4	I	Vref_3V3	CSI Data4 / GPIO5_22	
236	32K_OUT	ENET_RXD0	O	Vref_diff	32K Output / GPIO1_27	
237	LVDS0.CLK_P	LVDS0_CLK_P	O	Vref_diff	LVDS Clock+	
238	LVDS0.CLK_N	LVDS0_CLK_N	O	Vref_diff	LVDS Clock-	
239	LVDS0.TX0_P	LVDS0_TX0_P	O	Vref_diff	LVDS Transmit Data0+	
240	LVDS0.TX0_N	LVDS0_TX0_N	O	Vref_diff	LVDS Transmit Data0-	
241	GND		PWR	GND	Signal Ground	
242	LVDS0.TX1_P	LVDS0_TX1_P	O	Vref_diff	LVDS Transmit Data1+	
243	LVDS0.TX1_N	LVDS0_TX1_N	O	Vref_diff	LVDS Transmit Data1-	
244	LVDS0.TX2_P	LVDS0_TX2_P	O	Vref_diff	LVDS Transmit Data2+	
245	LVDS0.TX2_N	LVDS0_TX2_N	O	Vref_diff	LVDS Transmit Data2-	
246	LVDS0.TX3_P	LVDS0_TX3_P	O	Vref_diff	LVDS Transmit Data3+	
247	LVDS0.TX3_N	LVDS0_TX3_N	O	Vref_diff	LVDS Transmit Data3-	
248	Vref_diff		PWR	2V5	2.5V Voltage Reference	

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Pin No.	Signal Name	i.MX Ball Name	Type	Voltage Level	Function	Boot
249	CLK1.CLK_N	CLK1_N	O	Vref_diff	Clock1-	
250	CLK1.CLK_P	CLK1_P	O	Vref_diff	Clock1+	
251	PCIE.RX_N	PCIE_RXM	I	Vref_diff	PCIe Receive-	
252	PCIE.RX_P	PCIE_RXP	I	Vref_diff	PCIe Receive+	
253	PCIE.TX_N	PCIE_TXM	O	Vref_diff	PCIe Transmit-	
254	PCIE.TX_P	PCIE_TXP	O	Vref_diff	PCIe Transmit+	
255	EN_PERI	EIM_A25	O	Vref_3V3	Enable Signal for Peripheral Supply	
256	HDMI.HPD	HDMI_HPD	I	Vref_diff	HDMI Hot Plug Detect	
257	HDMI.DDCCEC	HDMI_DDCCEC	I/O	Vref_3V3	HDMI DDC/CEC	
258	Vref_3V3		PWR	3V3		
259	CSI0.DATA_EN	CSI0_DATA_EN	I	Vref_3V3	CSI Data Enable / GPIO5_20	
260	CSI0.PIXCLK	CSI0_PIXCLK	I	Vref_3V3	CSI Pixel Clock / GPIO5_18	
261	CSI0.HSYNC	CSI0_HSYNC	I	Vref_3V3	CSI Data Enable / GPIO5_19	
262	CSI0.VSYNC	CSI0_VSYNC	I	Vref_3V3	CSI Vertical Sync / GPIO5_21	
263	GND		PWR	GND	Signal Ground	
264	CSI0.D19	CSI0_D19	I	Vref_3V3	CSI Data19 / GPIO6_5	
265	CSI0.D18	CSI0_D18	I	Vref_3V3	CSI Data18 / GPIO6_4	
266	CSI0.D17	CSI0_D17	I	Vref_3V3	CSI Data17 / GPIO6_3	
267	CSI0.D16	CSI0_D16	I	Vref_3V3	CSI Data16 / GPIO6_2	
268	CSI0.D15	CSI0_D15	I	Vref_3V3	CSI Data15 / GPIO6_1	
269	Vref_3V3		PWR	3V3	3.3V Voltage Reference	
270	CSI0.D14	CSI0_D14	I	Vref_3V3	CSI Data14 / GPIO6_0	
271	CSI0.D13	CSI0_D13	I	Vref_3V3	CSI Data13 / GPIO5_31	
272	CSI0.D12	CSI0_D12	I	Vref_3V3	CSI Data12 / GPIO5_30	
273	CSI0.D11	CSI0_D11	I	Vref_3V3	CSI Data11 / GPIO5_29	
274	CSI0.D10	CSI0_D10	I	Vref_3V3	CSI Data10 / GPIO5_28	
275	Vref_diff		PWR	2V5	2.5V Voltage Reference	
276	LVDS1.CLK_N	LVDS1_CLK_N	O	Vref_diff	LVDS CLK-	
277	LVDS1.CLK_P	LVDS1_CLK_P	O	Vref_diff	LVDS CLK+	
278	LVDS1.TX0_N	LVDS1_TX0_N	O	Vref_diff	LVDS Transmit Data0-	
279	LVDS1.TX0_P	LVDS1_TX0_P	O	Vref_diff	LVDS Transmit Data0+	
280	LVDS1.TX1_N	LVDS1_TX1_N	O	Vref_diff	LVDS Transmit Data1-	
281	LVDS1.TX1_P	LVDS1_TX1_P	O	Vref_diff	LVDS Transmit Data1+	
282	LVDS1.TX2_N	LVDS1_TX2_N	O	Vref_diff	LVDS Transmit Data2-	
283	LVDS1.TX2_P	LVDS1_TX2_P	O	Vref_diff	LVDS Transmit Data2+	
284	LVDS1.TX3_N	LVDS1_TX3_N	O	Vref_diff	LVDS Transmit Data3-	
285	LVDS1.TX3_P	LVDS1_TX3_P	O	Vref_diff	LVDS Transmit Data3+	
286	DISP1.D13	EIM_A18	O	Vref_3V3	DISP Data13 / GPIO2_20	BOOT_CFG32
287	DISP1.D12	EIM_A17	O	Vref_3V3	DISP Data12 / GPIO2_21	BOOT_CFG31
288	DISP1.D11	EIM_EB0	O	Vref_3V3	DISP Data11 / GPIO2_28	BOOT_CFG43
289	DISP1.D10	EIM_EB1	O	Vref_3V3	DISP Data10 / GPIO2_29	BOOT_CFG44
290	DISP1.D9	EIM_DA0	O	Vref_3V3	DISP Data9 / GPIO3_0	BOOT_CFG10
291	DISP1.D8	EIM_DA1	O	Vref_3V3	DISP Data8 / GPIO3_1	BOOT_CFG11
292	DISP1.D7	EIM_DA2	O	Vref_3V3	DISP Data7 / GPIO3_2	BOOT_CFG12
293	GND		PWR	GND	Signal Ground	
294	DISP1.D6	EIM_DA3	O	Vref_3V3	DISP Data6 / GPIO3_3	BOOT_CFG13
295	DISP1.D5	EIM_DA4	O	Vref_3V3	DISP Data5 / GPIO3_4	BOOT_CFG14

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Pin No.	Signal Name	i.MX Ball Name	Type	Voltage Level	Function	Boot
296	DISP1.D4	EIM_DA5	O	Vref_3V3	DISP Data4 / GPIO3_5	BOOT_CFG15
297	DISP1.D3	EIM_DA6	O	Vref_3V3	DISP Data3 / GPIO3_6	BOOT_CFG16
298	DISP1.D2	EIM_DA7	O	Vref_3V3	DISP Data2 / GPIO3_7	BOOT_CFG17
299	DISP1.D1	EIM_DA8	O	Vref_3V3	DISP Data1 / GPIO3_8	BOOT_CFG20
300	DISP1.D0	EIM_DA9	O	Vref_3V3	DISP Data0 / GPIO3_9	BOOT_CFG21

Table 4-3: Connector description X3

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5 Application Information

5.1 Supply Voltage Decoupling

For better stability we recommend to add a 100nF capacitor to each power supply pin and an additional 47µF tantalum capacitor to the V_{IN} voltage rail next to the module.

5.2 Power Outputs

For better stability we recommend to add a 100nF capacitor to each used power output pin and an additional 2.2µF tantalum capacitor to each voltage rail next to the module.

5.3 Peripheral Supply

NOTE: **EN_PERI** (Pin 255) indicates when the base board is permitted to power its peripherals. Do not power your peripherals until this signal line is high, otherwise the SoM can be seriously damaged! When EN_PERI is active (high) the SoM has powered up properly and all of the required power lines are available.
The EN_PERI signal should be used to enable the power supplies or power gates on the base board.

5.4 Reset circuit

The pin CTRL.nRESET_IN can be used to reset the i.MX6x. CTRL.nRESET_IN is pulled high by 30kΩ to Vref_5V0 on the SoM. This pin can therefore be connected to an open-drain signal or to a push-button that connects CTRL.nRESET_IN to GND.

Asserting CTRL.nRESET_IN will reset all internal modules and logic of the i.MX6x. After CTRL.nRESET_IN is released, the i.MX6x reads the boot configuration from CTRL.BM0 and CTRL.BM1 and starts the boot procedure.

5.5 Differential pairs

All signals/pins named *_N/*_P (for example: LVDS1.CLK_N and LVDS1.CLK_P) are differential pairs which should be routed with a differential impedance listed in Table 5-1 for a good signal integrity and to prevent EMI problems.

Differential Pair	Differential impedance [Ω]	Differential Pair	Differential impedance [Ω]
CLK1	100	**PCIE.RX**	85
CLK2	100	**PCIE.TX**	85
GETH.TXRX_A	100	**HDMI.CLK**	100
GETH.TXRX_B	100	**HDMI.D0**	100
GETH.TXRX_C	100	**HDMI.D1**	100
GETH.TXRX_D	100	**HDMI.D2**	100
CSI.CLK	100	**LVDS0.CLK**	100
CSI.D0	100	**LVDS0.TX0**	100
CSI.D1	100	**LVDS0.TX1**	100
CSI.D2	100	**LVDS0.TX2**	100
CSI.D3	100	**LVDS0.TX3**	100
DSI.CLK	100	**LVDS1.CLK**	100

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Differential Pair	Differential impedance [Ω]	Differential Pair	Differential impedance [Ω]
DSI.D0	100	**LVDS1.TX0**	100
DSI.D1	100	**LVDS1.TX1**	100
SATA.RX	100	**LVDS1.TX2**	100
SATA.TX	100	**LVDS1.TX3**	100
USB_H.D	90	**USB_OTG.D**	90

Table 5-1: Differential impedances

5.6 Single-ended signals

All signals which are not differential pairs should be routed with a single ended impedance of 50Ω to minimize EMI.

5.7 Application Example Schematics

Have a look at our XYZDEV-BF5xx (TBD) schematics, which can be found at http://www.bluetechnix.com/goto/XYZ (TBD) to get application examples.

Preliminary

6 Mechanical Outline

6.1 Top View

Figure 6-1 shows the top view of the mechanical outline of the CM-i.MX6 SoM. All dimensions are given in millimeters! Outline dimensions +/- 0.5mm.

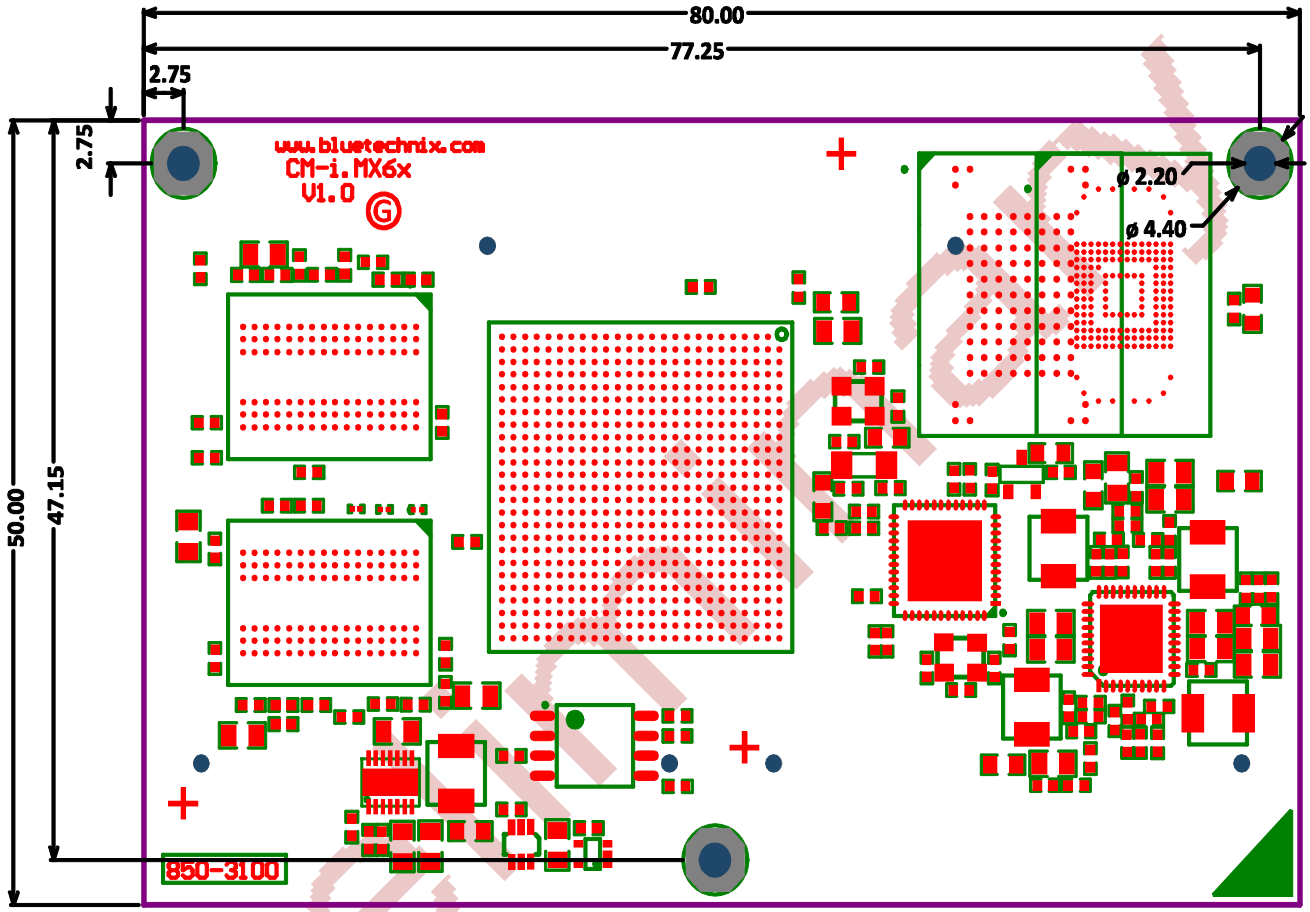

Figure 6-1: Mechanical outline (top view)

6.2 Bottom View

Figure 6-2 shows the top view of the mechanical outline of the CM-i.MX6 SoM. All dimensions are given in millimeters! Outline dimensions +/- 0.5mm.

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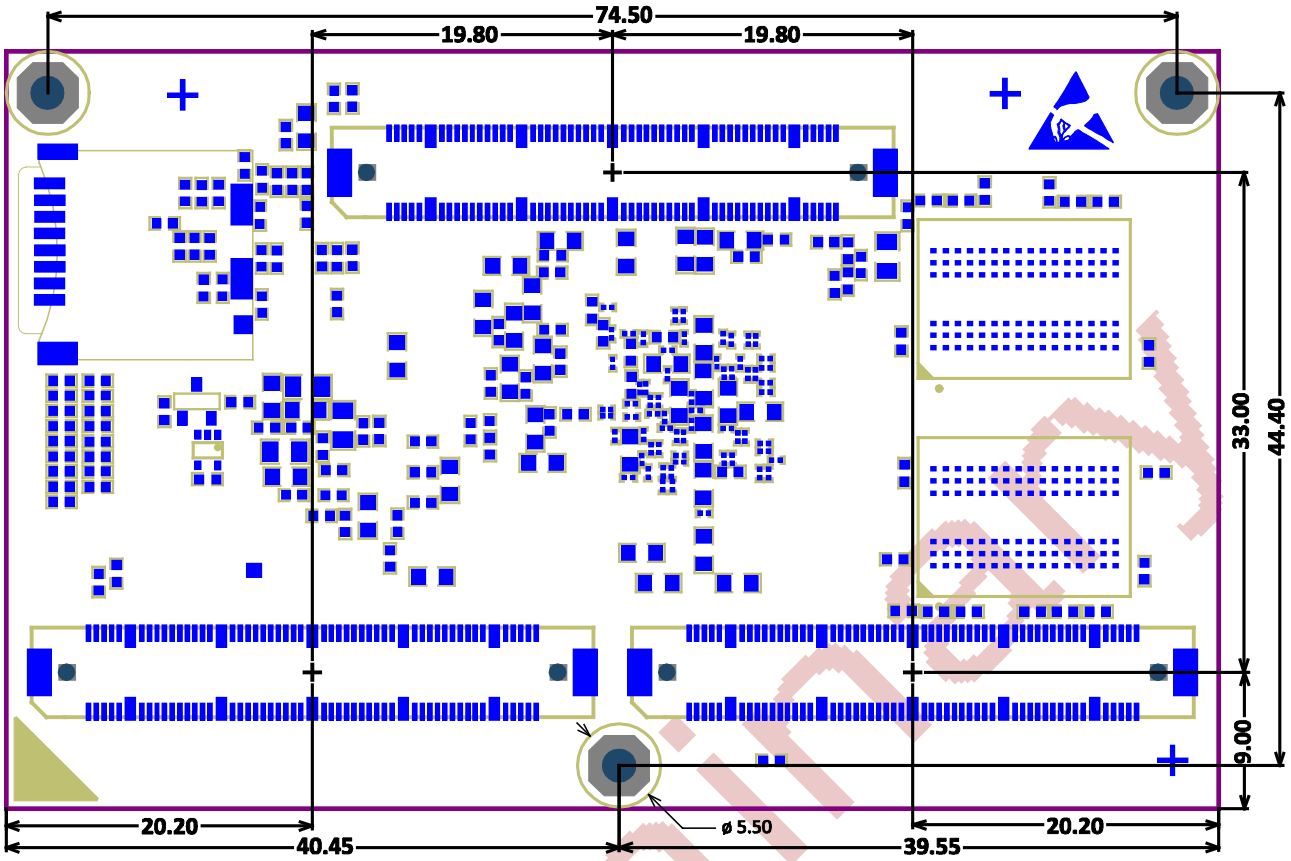

Figure 6-2 Mechanical outline (bottom view)

6.3 Side View

Figure 6-3 shows the mechanical outline of the side of the CM-i.MX6x SoM. All dimensions are given in millimeters! Outline dimensions +/- 0.5mm.

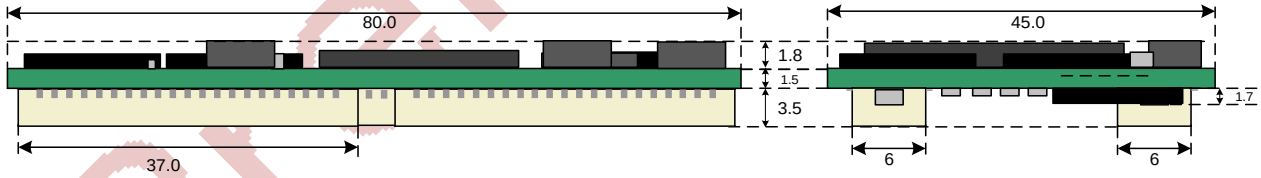

Figure 6-3: Mechanical outline (side view)

Contact Bluetechnix GmbH Support for a detailed STEP model.

6.4 Footprint

Figure 6-4 shows the footprint (top view) of the CM-i.MX6 SoM. All dimensions are given in millimeters!

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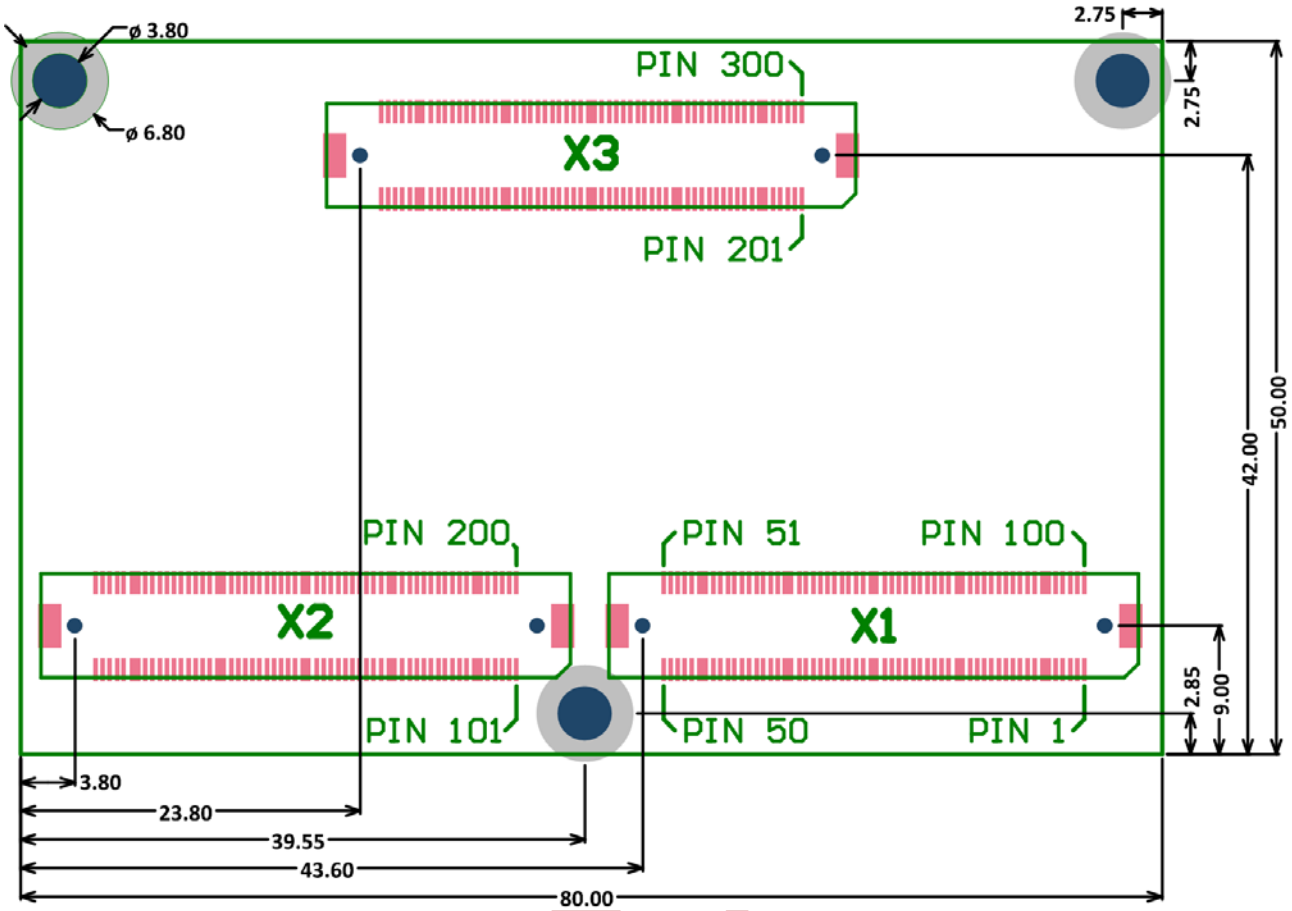

Figure 6-4: Footprint (top view)

The footprint for Altium Designer is available on request. The used connector is FX-10A-100S/10SV from Hirose. For detailed dimensions of the connectors please see the datasheet from the manufacturer's web site.

The mounting holes are designed for reflow solderable spacers SMTSO-M2-4 from PEM. For further details regarding dimensions and paste expansion please refer to the manufacturer's website. If simple holes are desired on the base board, identical ones as on the SoM are recommended.

6.5 Connectors

Connector SoM	Manufacturer	Manufacturer Part No.	Matching Connector
X1	Hirose	FX-10A-100P/10SV	FX-10A-100S/10SV
X2	Hirose	FX-10A-100P/10SV	FX-10A-100S/10SV
X3	Hirose	FX-10A-100P/10SV	FX-10A-100S/10SV

Table 6-1: SoM connector types

The SoM features 3 connectors. The base board has to use the opposite connectors (FX-10A-100S/10SV).

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7 Support

7.1 General Support

General support for products can be found at Bluetechnix' support site https://support.bluetechnix.at/wiki

7.2 Board Support Packages

Board support packages, boot loaders and further software downloads can be downloaded at the Products wiki page at https://support.bluetechnix.at/software/

7.3 i.MX Software Support

7.3.1 Linux

Linux BSP and images of derivates can be found at Bluetechnix' support site https://support.bluetechnix.at/wiki at the software section of the related product.

7.3.2 Android

~~WinCE is only supported on ARM platforms.~~ Please contact Bluetechnix for support information.

7.3.3 Win CE

~~WinCE is only supported on ARM platforms.~~ Please contact Bluetechnix for support information.

7.4 i.MX Design Services

Based on more than seven years of experience with Blackfin and i.MX, Bluetechnix offers development assistance as well as custom design services and software development.

7.4.1 Upcoming Products and Software Releases

Keep up to date with all product changes, releases and software updates of Bluetechnix at http://www.bluetechnix.com.

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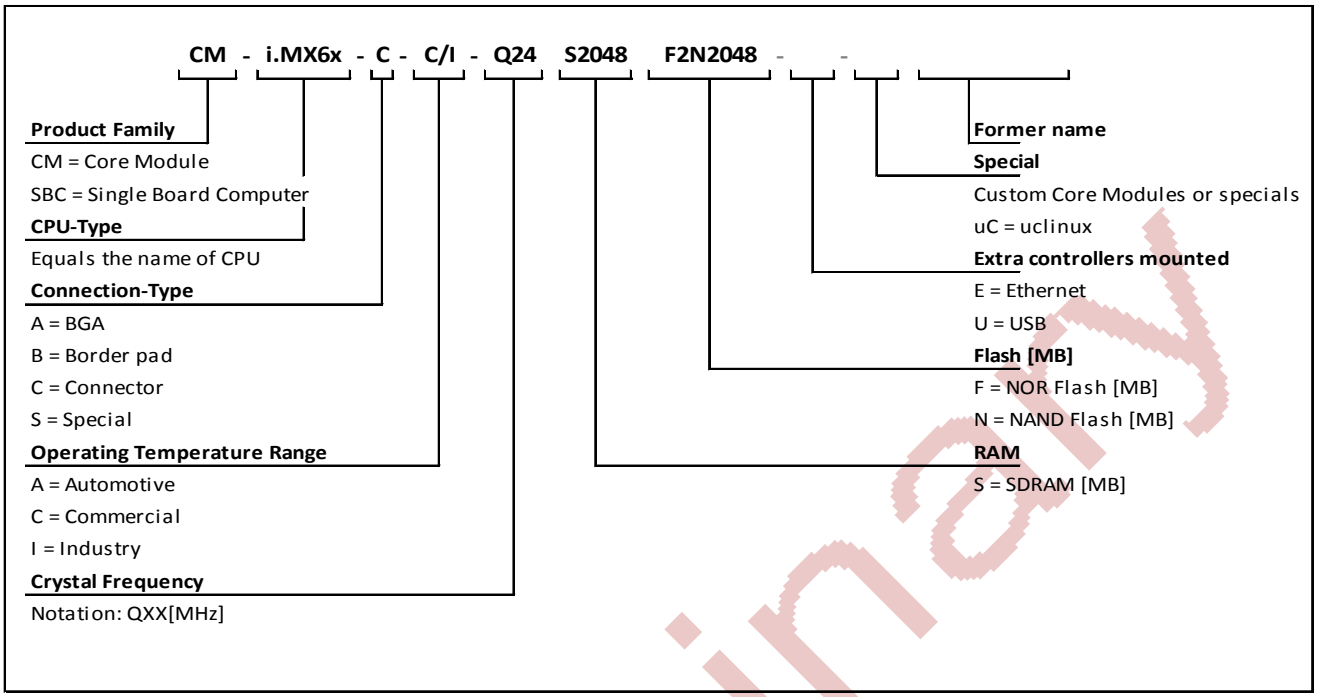
8 Ordering Information



8.1 Predefined mounting options for CM-i.MX6x

Article Number	Name	Nick name	Temperature Range
100-1480-1	CM-i.MX6Q-C-I-Q24S2048F2N2048	CM-i.MX6Q Industrial	Industrial
100-1481-1	CM-i.MX6Q-C-C-Q24S2048F2N2048	CM-i.MX6Q	Commercial
100-1482-1	CM-i.MX6D-C-I-Q24S2048F2N2048	CM-i.MX6D Industrial	Industrial
100-1483-1	CM-i.MX6D-C-C-Q24S2048F2N2048	CM-i.MX6D	Commercial

Table 8-1: Ordering information

NOTE: Custom SoMs are available on request! Please contact Bluetechnix (office@bluetechnix.com) if you are interested in custom SoMs.

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9 Dependability

9.1 MTBF

Please keep in mind that a part stress analysis would be the only way to obtain significant failure rate results, because MTBF numbers just represent a statistical approximation of how long a set of devices should last before failure. Nevertheless, we can calculate an MTBF of the SoM using the bill of material. We take all the components into account. The PCB and solder connections are excluded from this estimation. For test conditions we assume an ambient temperature of 30°C of all SoM components except the Blackfin® processor (80°C) and the memories (70°C). We use the MTBF Calculator from ALD (http://www.aldservice.com/) and use the reliability prediction MIL-217F2 Part Stress standard. Please get in touch with Bluetechnix (office@bluetechnix.com) if you are interested in the MTBF result.

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10 Product History

10.1 Version Information

10.1.1 CM-i.MX6Q-C-C-Q24S2048F2N2048 (CM-i.MX6Q)

Version	Component	Type
1.0.0	Processor	MCIMX6Q5EYM10AC
	RAM	MEM4G16D3EABG (512MB)
	Flash	H26M21001FPR (2GB)

Table 10-1: Overview CM-iMX6x product changes

10.2 Anomalies

Version	Date	Description
V1.0	2012 12 19	No anomalies reported yet.

Table 10-2 – Product anomalies

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11 Document Revision History

Version	Date	Document Revision
1	2012 12 19	First release V1.0 of the Document

Table 11-1: Revision history

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12 List of Abbreviations

Abbreviation	Description
ADI	Analog Devices Inc.
AI	Analog Input
AMS	Asynchronous Memory Select
AO	Analog Output
CM	Core Module
DC	Direct Current
DSP	Digital Signal Processor
eCM	Enhanced Core Module
EBI	External Bus Interface
ESD	Electrostatic Discharge
GPIO	General Purpose Input Output
I	Input
I²C	Inter-Integrated Circuit
I/O	Input/Output
ISM	Image Sensor Module
LDO	Low Drop-Out regulator
MTBF	Mean Time Between Failure
NC	Not Connected
NFC	NAND Flash Controller
O	Output
OS	Operating System
PPI	Parallel Peripheral Interface
PWR	Power
RTOS	Real-Time Operating System
SADA	Stand Alone Debug Agent
SD	Secure Digital
SoC	System on Chip
SoM	System-on-Module
SPI	Serial Peripheral Interface
SPM	Speech Processing Module
SPORT	Serial Port
TFT	Thin-Film Transistor
TISM	Tiny Image Sensor Module
TSC	Touch Screen Controller
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
USBOTG	USB On The Go
ZIF	Zero Insertion Force

Table 12-1: List of abbreviations

PRELIMINARY

A List of Figures and Tables

Figures

Tables

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