BLUE TECHNIX

Hardware User Manual

CM-i.MX31 V1.x

...maximum performance at minimum space

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Warning

Due to technical requirements components may contain dangerous substances.

The Core Modules and development systems contain ESD (electrostatic discharge) sensitive devices. Electro-static charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused Core Modules and Development Boards should be stored in the protective shipping

1 Introduction

The CM-i.MX31 is a tiny, high performance and low power ARM1136JF-S based Core Module incorporating Freescale's high performance i.MX Processor. The CM-i.MX31 is available in Connector and Ball Grid Array (BGA) versions. The BGA version offers a lower overall cost and is optimized for mobile devices where mounting height is limited. If Ethernet functionality is required, it can be provided on the baseboard.

The connector version comes with an SMSC Ethernet controller and is used for development or final application purposes. For series production, the BGA or connector versions can be used.

The special feature of this module is the high flexibility in different mounting configurations (Consult the Mounting Options section) thus lowering the overall cost without costly redesign.

The CM-i.MX31 (Connector or BGA) is designed for mobile battery powered applications and to our knowledge it is the world's smallest Core Module of its kind.

1.1 Overview

The Core Module CM-i.MX31 consists of the following components:

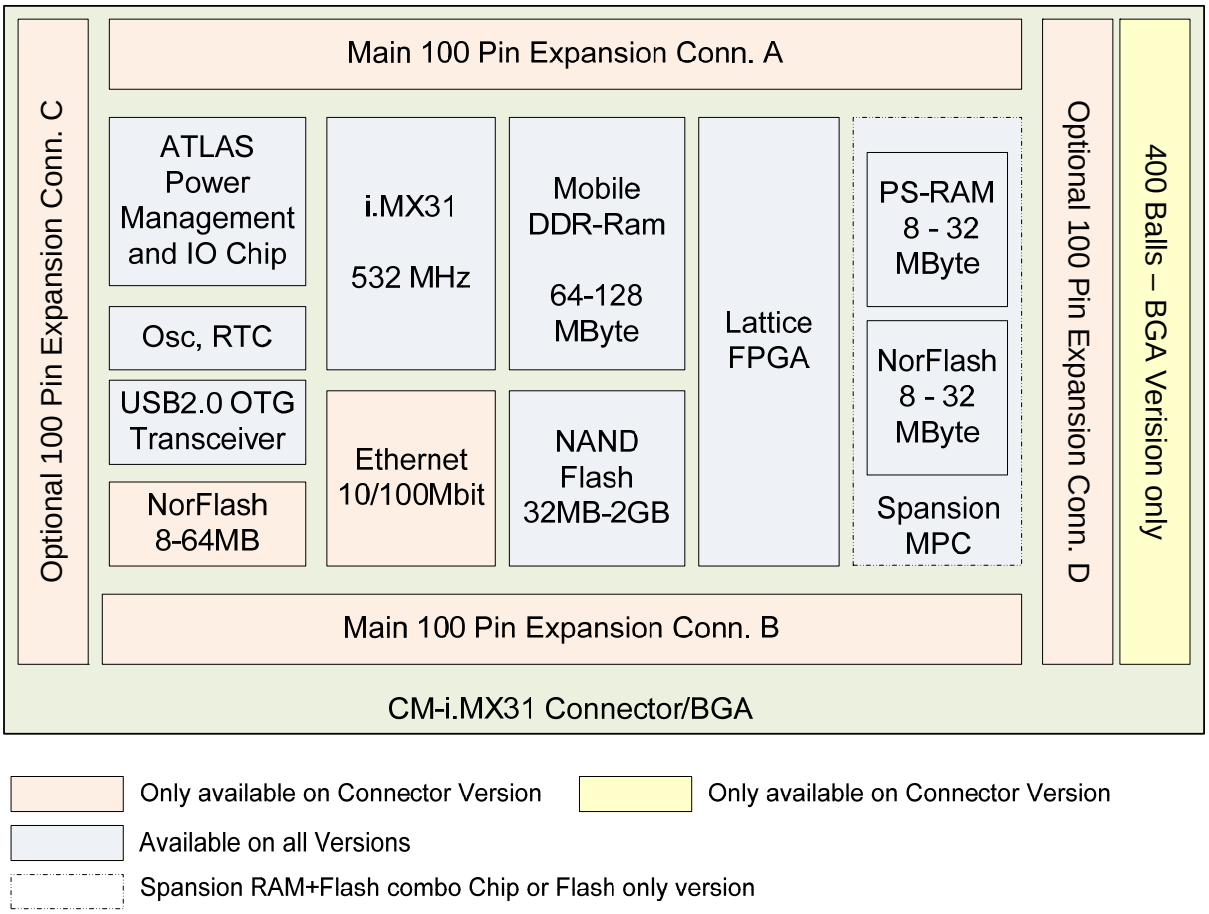

Figure 1-1: Main components of the CM-i.MX31 Core Module

1.1.1 Freescale i.MX31L Processor

Functions:

- Connectivity (internal)
  - 3 CSPI
  - 2 SSI/I2S
  - 3 I2C
  - AUDMUX
- Connectivity (external)
  - 5 UART
  - USB OTG HS
  - 2 USB Host
  - 1-Wire interface
  - Fast IrDA
- Expansion
  - 2 MMC/SD
  - PCMCIA/CF
  - 2 Memory Stick – Pro
  - SIM
  - ATA
- Memory interface
  - SDRAM/DDR
  - PSRAM
  - SmartMedia
- Standard system I/O
  - SDMA
  - 3 Timers
  - PWM
  - WD Timer
  - RTC
  - GPIO
  - RAM, ROM
- Image processing unit
  - Inversion and Rotation
  - Camera I/F
  - Blending
  - Display/TV Ctrl
  - Pre and post processing
- Multimedia and human interface
  - Graphics accelerator (only available in i.MX31)
  - MPEG-4 Encoder
  - Keypad
- System control
  - JTAG, ETM
  - Bootstrap
  - System Reset
  - PLL
  - Power Management
- CPU complex
  - ARM1136 CPU

- Smart Speed Switch (MAX)
- 16Kbytes I-Cache
- 16Kbytes D-Cache
- 128Kbytes L2-Cache
- ROM Patch
- ETM
- Vector Floating Processor

Supported Chips:

- i.MX31L
- i.MX31

1.1.2 Freescale ATLAS MC13783 Companion Chip

Energy Management

- Optimized power distribution to increase battery life
  - linear regulators
  - two buck switchers with DVS control
  - One boost switcher
- Ultra low dropout voltage regulator (200mV)
- Switcher frequency adjustment to reduce RF spurious
- Regulators are fully controlled by processors
- Integrated protections (current and temperature)
- Power-up sequencer
- Low-power standby mode
- Integrated multimode charger
  - Trickle, linear, pulse and USB charging modes
  - Accessories supply mode (bottom plug)
  - Charge current controlled by SPI
  - Current and voltage monitored by ADC
  - Overvoltage protections

Audio Interfacing

- Audio Inputs
  - Three amplified inputs and bias for microphone
  - Stereo input for external stereo
- Audio Outputs
  - High-power differential amplifier for earpiece/hands free/polyphonic music
  - Two single-ended amplifiers for stereo headset
  - Earpiece amplifier
- Voice Codec
  - 13-bit linear Tx and Rx mode
  - 8kHz and 16kHz supported
  - Additional ADC for stereo or noise cancellation
- Stereo DAC
  - 16-bit linear/multirate, multiclock modes (PLL)
  - Network mode supported (four slots)
- Audio buses interface
  - Two interchangeable SSI buses
  - Master/slave mode supported

System Control

- On/off phone power cycling
    - On/off state machine
    - Power-up events (on/off switch buttons, alarms)
    - Power-off events (watchdog failure, OV, UV, temperature)
- Reset
    - System RST output
    - MCU RST for warm start
    - Warm/cold start flag
- Specific power modes (for battery life optimization)
    - Memory hold mode
    - User off mode

Analog Sensor Control

- 10-bit ADC
- Four-wire resistive touch-screen interface with state machine
- Thermal bias (battery)
- Eight internal sense channels (including voltage and current reading on battery and charger)
- Fully controlled via SPI
- Programmable digital comparators

Wired connectivity

- USB Transceiver
    - USB 2.0 compatible, LS and FS supported
    - USB-OTG supported
    - USB boot mode
- RS-232 Transceiver
    - Multiplexed with USB
    - RS-232 boot mode
- Bottom Connector
    - Option for separate pins for USB power and charger
    - Multiplexed RS-232 and USB data pins
    - Includes analog audio routing via D+ and D- lines

Peripherals

- Lighting
    - Three backlight drivers for LCDs and keypad
    - Programmable level and PWM control
    - Three sets of RGB tricolor LED drivers
    - Programmable level and PWM control
- Signaling
    - Vibrator interface

Clocks and timing

- Clocks
    - 32kHz system clock
    - Two clock outputs with different voltage domain
- Real-Time-Clock

- Time and date
- Alarm including phone wake-up functions
- Timebase by crystal oscillator
- System timekeeping
- Supply backup by coin cell
- RC mode until crystal is stabilized

Current Consumption

- Standby mode (RTC and regulators into low-power mode): 140µA
- Off mode (RTC and core logic): 30µA
- RTC only: 5µA

1.1.2.1 Mobile DDR-SDRAM

- 2x MT46H32M16LFCK-6 (512Mbit) **(default)**
- 2x MT46H16M16LFCK-6 (256Mbit) (optional)
- Different DDR SDRAM options available upon request

1.1.2.2 Spansion MCP (Multi-Chip Product)

- S71WS256ND0BFWYP0 **(default)**
  - 32MB Flash: 16Mx16 (256Mbit)
  - 16MB PS-RAM: 8Mx16 (128Mbit)
- S29WS256NOSBFW010 (optional)
  - 32MB Flash: 16Mx16 (256Mbit)
- Different Spansion MCP options available upon request

1.1.2.3 NAND Flash

- NAND01GW3B2AZA6E (**default**)
  - 128Mx8 (1Gbit), 3.3V IO Voltage
- Different NAND Flashes in FBGA63 package available upon request. Micron, Samsung, ST Microelectronics.

1.1.2.4 Intel Strata Boot Flash (on Connector Version only)

- PF48F2000P0ZBQ0 (**default**)
  - 8MB Flash: 32Mx16 (64Mbit)
- Different Flash sizes available upon request

1.1.2.5 10/100Mbit Ethernet Controller (on Connector Version only)

- SMSC LAN9211 (**default**)
- SMSC LAN9210

1.1.2.6 FPGA

- Lattice LATLCMXO256C-5MN100C FPGA based 3V3 Level shifter and Address decoder for D&A Bus
- Alternative FPGA implementations possible.

1.2 Target Applications

- Industrial PDA
- Medical Devices
- Low cost point of sale terminal module
- Generic high performance multimedia processor module
- Multimedia Application Processor Module
- Internet Connected Embedded System

2 Specification

2.1 Functional Specification

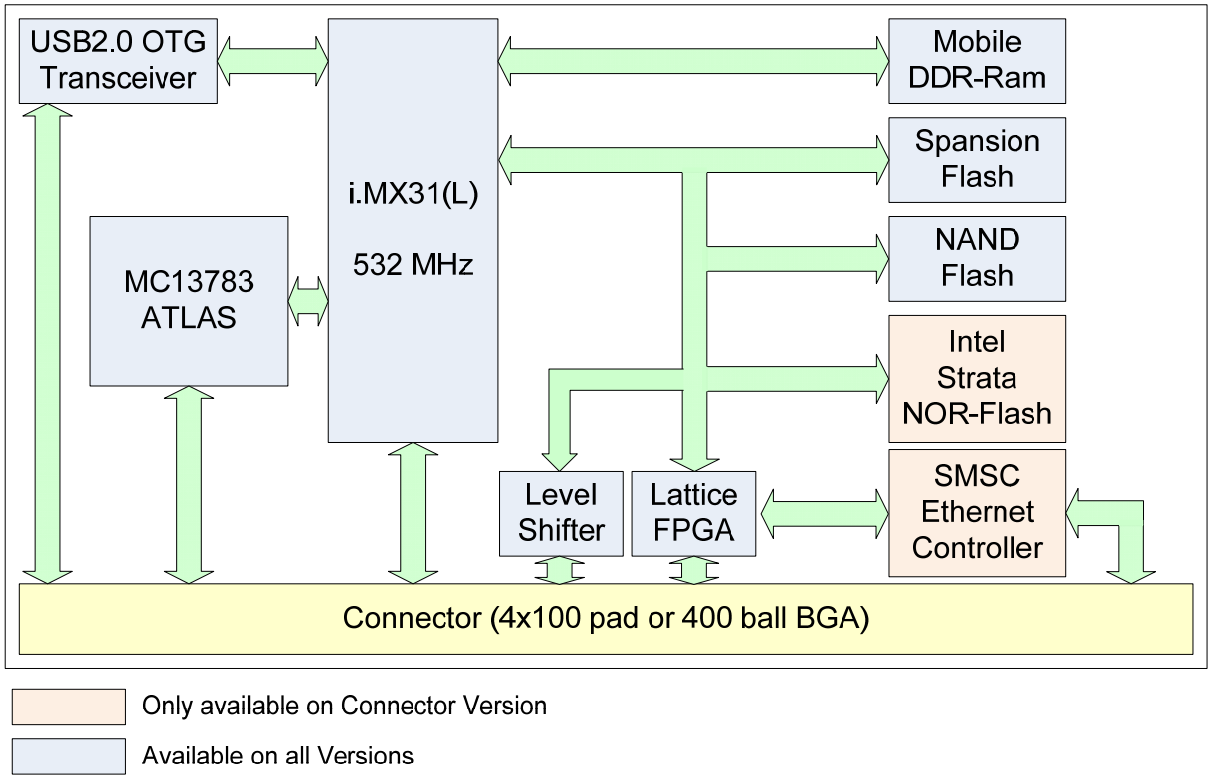

Figure 2-1: Detailed Block Diagram

Figure 2-1 shows a detailed block diagram of the CM-i.MX31 Core Module.

2.2 Boot Mode

The Core Module supports several boot modes. Table 2-1 shows the different boot modes and their boot functions. 0 is the logical low voltage level and a 1 stands for the logical high level. The voltage domain from the boot mode pins is NVCC1. For special information about the boot modes take a look at the reference manual from the MCIMC31.

BM4	BM3	BM2	BM1	BM0	Function
0	0	0	0	0	UART/USB boot loader int
0	0	0	0	1	8-bit NAND Flash (2 Kbytes per page)
0	0	0	1	0	8-bit NAND Flash (512 bytes per page)
0	0	0	1	1	16-bit NAND Flash (2 Kbytes per page)
0	0	1	0	0	16-bit NAND Flash (512 bytes per page)
0	0	1	0	1	16-bit CS0 at D[15:0]
0	0	1	1	0	reserved
0	0	1	1	1	reserved
0	1	0	0	0	M-Systems Disk On Chip
0	1	0	0	1	reserved
0	1	0	1	0	reserved
0	1	0	1	1	reserved

BM4	BM3	BM2	BM1	BM0	Function
0	1	1	0	0	reserved
0	1	1	0	1	reserved
0	1	1	1	0	reserved
0	1	1	1	1	reserved
1	0	0	0	0	8-bit NAND Flash (2 Kbytes per page)
1	0	0	0	1	8-bit NAND Flash (512 bytes per page)
1	0	0	1	0	16-bit NAND Flash (2 Kbytes per page)
1	0	0	1	1	16-bit NAND (512 bytes per page)
1	0	1	0	0	16-bit CS0 at D[15:0]
1	0	1	0	1	reserved
1	0	1	1	0	reserved
1	0	1	1	1	reserved
1	1	0	0	0	reserved
1	1	0	0	1	reserved
1	1	0	1	0	reserved
1	1	0	1	1	reserved
1	1	1	0	0	reserved
1	1	1	0	1	reserved
1	1	1	1	0	reserved
1	1	1	1	1	reserved

Table 2-1: Boot Modes

2.3 EMI Memory map

The EMI supports 4 different memory controllers. Table 2-2: Memory Map illustrates the memory map for the default board configuration.

Memory Type	Start Address	End Address	Size	i.MX CS	Comment
DDR SD-RAM	0x8000'0000	0x8FFF'FFFF	128MB	CSD0	2x16bit Micron DDR
Spansion Flash	0xA000'0000	0xA1FF'FFFF	32MB	CS0	16bit Bus, Spansion MCP (default Boot Flash)
Spansion Flash	0xA800'0000	0xA9FF'FFFF	32MB	CS1	16bit, Spansion MCP extended Flash size (not default!)
Intel Strata P30/P33 Flash	0xA800'0000	0xA87F'FFFF	8MB	CS1/ CS0	Optional only on connector version, CS1 default, CS0 optional
Spansion PS-RAM	0xB600'0000	0xB6FF'FFFF	16MB	CS5	16bit Bus, Spansion MCP
FPGA CS1	0xB200'0000	0xB3FF'FFFF	32MB	CS3	For details see FPGA section
FPGA CS2	0xB400'0000	0xB5FF'FFFF	32MB	CS4	For details see FPGA section

Table 2-2: Memory Map

2.4 Power Domains

Table 2-3 shows to which power-source each domain is connected.

Domain on MXIMC31	Power	Voltage (V)
QVCC_PER	P_SW1	0.900 - 1.675 in 25 mV steps, 1.700 - 2.200 in 100 mV steps
NVCC1, NVCC2, NVCC3, NVCC10, FUSE VDD	P_SW2	0.900 - 1.675 in 25 mV steps, 1.700 - 2.200 in 100 mV steps
NVCC5, NVCC6, NVCC7, NVCC9	P_VRF1	2.475/2.60/2.700/2.775
NVCC4, NVCC8	P_VIOHI	2.775
XVCC	P_VDIG	1.2/1.5/1.8/1.875

Table 2-3: Power Domain Map

For detailed information take a look at the MC13786 (ATLAS) user guide and the MCIMX31 reference manual.

The default preconfigured power up sequence on the Core Module is PUMS[3..1] = [HI, open, LO]. See the following table for the exact supply voltage. If you need another power up sequence or default voltages, you have to change the mount options (see chapter **Error! Reference source not found.**).

Domain on MCIMX31	Power	Default Voltage Level
QVCC_PER	P_SW1	1.6V
NVCC1, NVCC2, NVCC3, NVCC10, FUSE_VDD	P_SW2	1.8V
NVCC5, NVCC6, NVCC7, NVCC9	P_VRF1	2.775V
NVCC4, NVCC8	P_VIOHI	2.775
XVCC	P_VDIG	1.875
-	P_VAUDIO	2.775V
-	P_VIOLO	1.8V
-	P_VRFREF	2.775V
-	P_VSIM	off
-	P_VESIM	off
-	P_VGEN	1.5V
-	P_VCAM	2.8V
-	P_VRF2	2.775V
-	P_VMCC1	2.8V
-	P_VMCC2	2.8V

Table 2-4: Default Voltage Levels

For more information about the power up sequence and default voltage levels see the MC13783 user guide.

2.5 Reset Domains

2.5.1 RESET_B

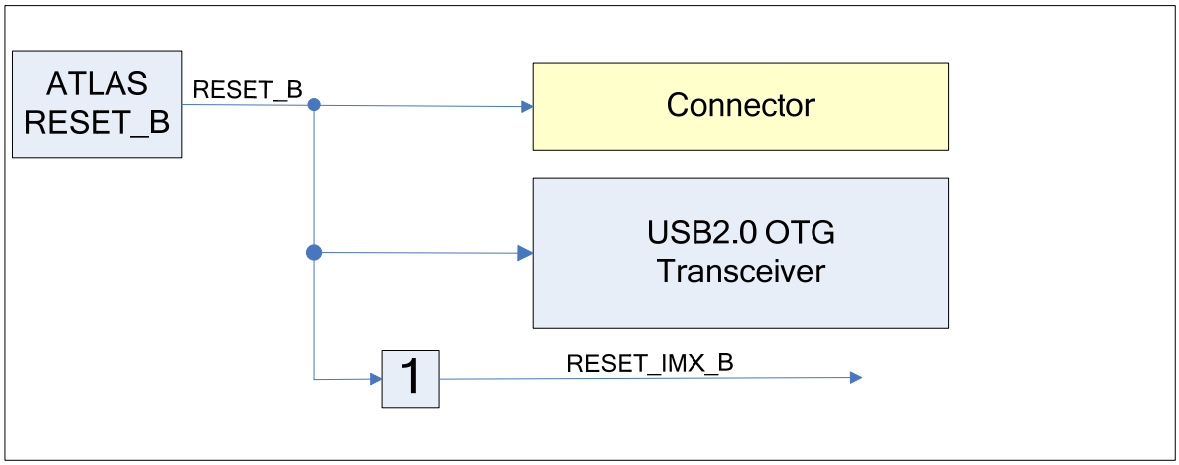

Figure 2-2 Block Diagram for RESET_B

2.5.2 RESET_IMX_B

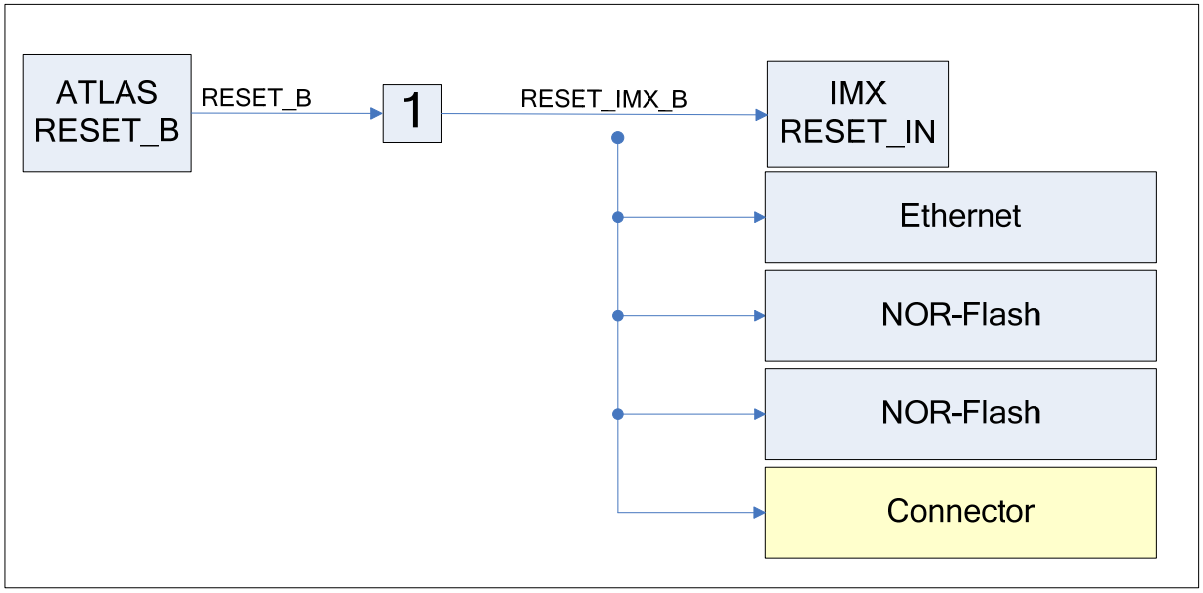

Figure 2-3: Block Diagram for RESET_IMX_B

2.5.3 RESETB_MCU

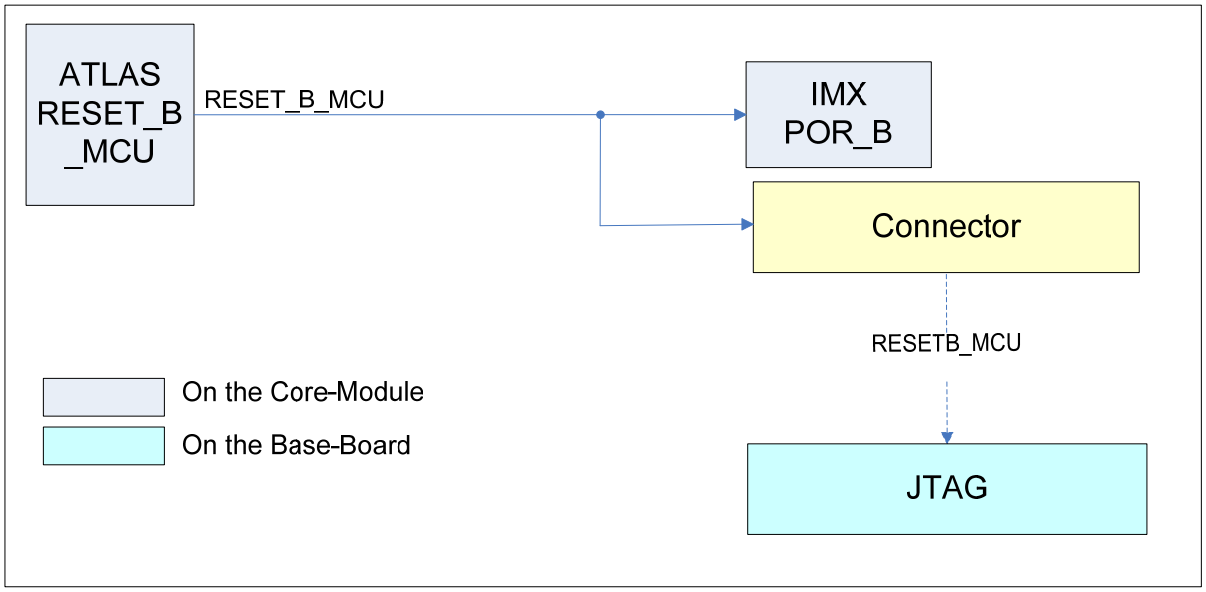

Figure 2-4: Block Diagram for RESETB_MCU

2.6 Clock Signals

The Figure 2-5 gives an overview of the clock signal distribution on the Core Module. The USB-OTG transceiver is the main clock source for the 26MHz. The i.MX31 master clock is connected to this source as well as the Atlas digital audio interface clocks (CLIA, CLIB). If the i.MX needs another Input clock, e.g. 27MHz for analogue video applications, you have to do some soldering on the Core Module. Please contact bluetechix for more information.

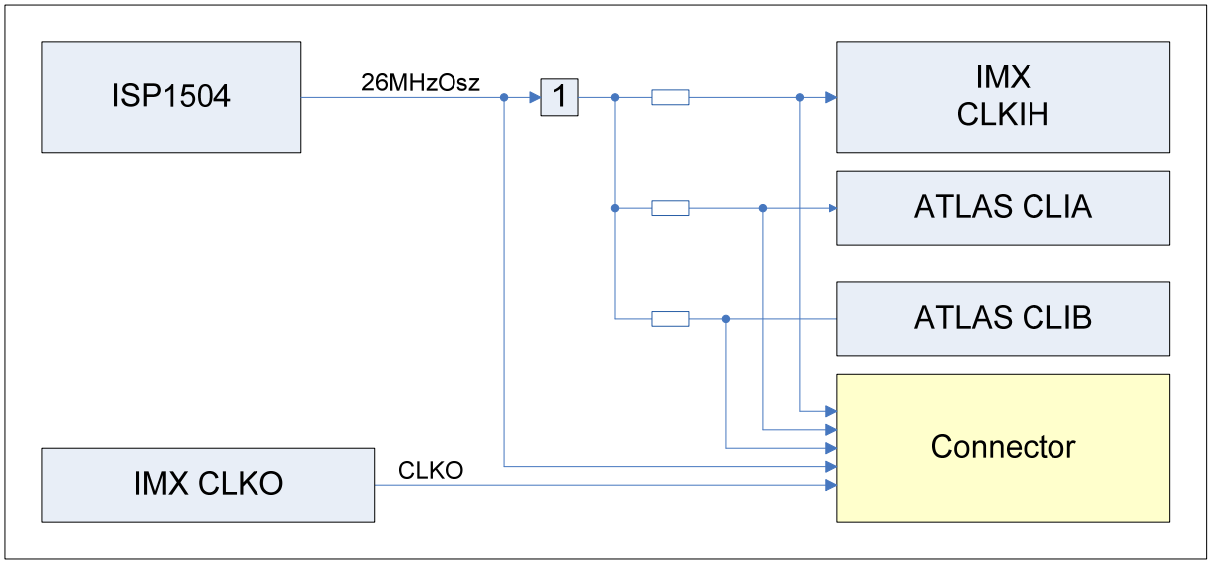

Figure 2-5: Clock signal distribution

2.7 Core Module Supply

Figure 2-6 gives an overview, of the power domains on the CM-i.MX31. The battery charger and the voltage regulators are all integrated in the MC13783 (Atlas) IC. If you need more information about this topic please refer to the MC13783 user guide.

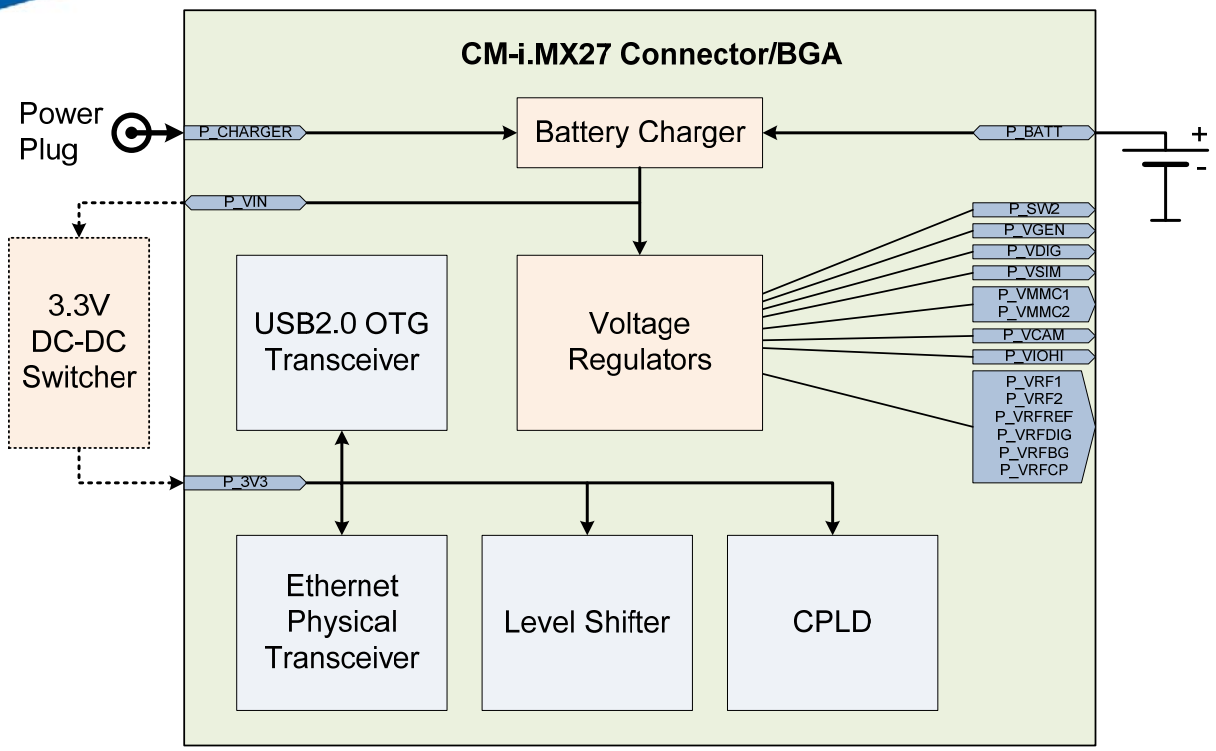

Figure 2-6: Core Module Power

There are two possibilities to power the Core Module. For mobile devices it is recommended to connect a Li-Ion battery to the P_BATT pins to supply the module. When an AC/DC wall adapter is connected to P_CHARGER the battery will be charged. The module works also, if there is no battery connected (or the battery is broken), but the wall adapter is still connected (**dead battery mode**).

Note that the module won't work without external 3.3V supply. In this mode (see Figure 2-6) the 3V3 voltage generator could be sourced with the P_VIN coming from the module.

The second way to power the module is to connect the P_VIN and P_3V3 pins together to an external 3.3V stabilized power supply. P_CHARGER must remain unconnected!

2.8 Electrical Specification

2.8.1 Supply Options

- P_3V3: 3.135V – 3.465V
- Li-Ion Battery 2.8-4.65V +/-10%
- Coin cell Voltage (LICELL): 2.5V to 3.3V
- P_CHARGER: 5V to 20V (e.g. AC/DC Wall adapter as charger)

2.8.2 Charger Current

The charger current should not exceed 300mA without heat sink and 1A with heat sink (P_CHARGE=5V and T_{amb}=25°C).

2.8.3 Supply Current

The maximum supply current depends heavily on your application and how the module is powered (P_CHARGER, P_BATT, P_3V3).

As an average value for power consumption in normal operation (e.g. PDA functionality) 1.7W can be assumed.

2.9 Environmental Specification

2.9.1 Temperature

- Storage temperature: -40° to 125°C
- Operating temperature: +0 to + 70° C or -40 to +85°C (see Variants)

2.9.2 Humidity

Operating: 10% to 90% (non condensing)

3 CM-i.MX31C (Connector Version)

3.1 Mechanical Outline

All dimensions are given in millimetres!

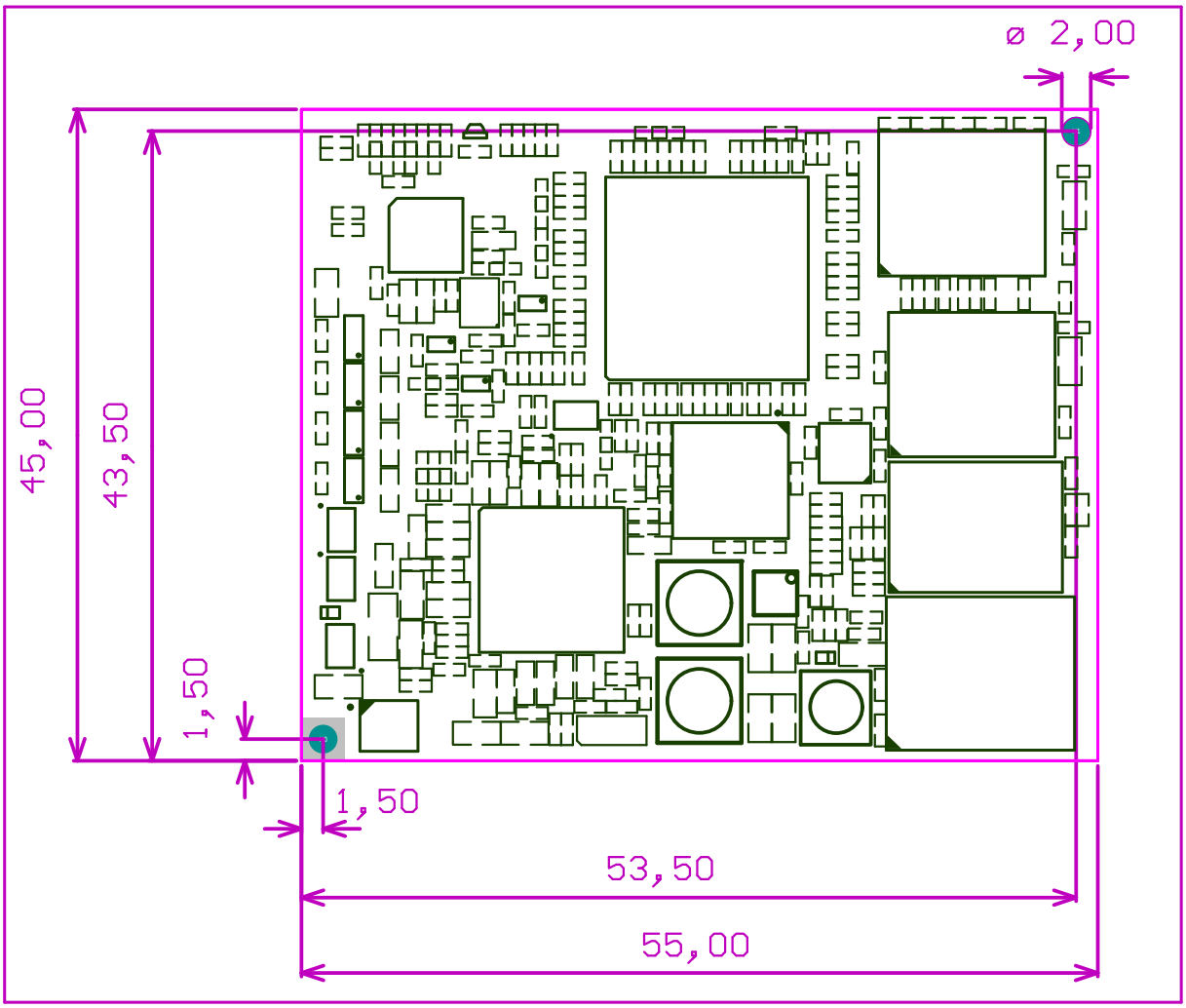

Figure 3-1: Mechanical outline (top view)

The mechanical outline represents a top view; the connectors are placed at the bottom side of the Core Module.

Due to scoring tolerances in the PCB production the Board outline can increase by max. 0.5mm on each side.

The module is shipped either with two 100pin connectors (main connectors) or with four 100pin connectors (**default**) if additional interfaces are required.

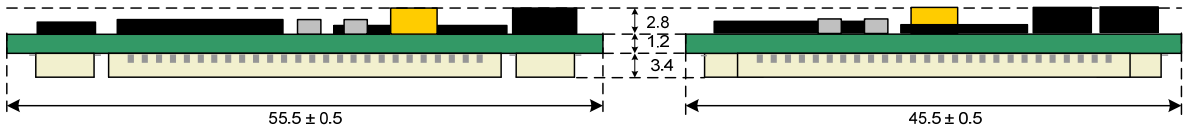

Figure 3-2: Side View with Connector mounted

The total minimum mounting height from the baseboard is 8mm, the stacking height (board to board spacing) is 4mm.

Note: It is not recommended to place parts under the Core Module!

3.2 Footprint of Connector Version

For the baseboard the following connectors have to be used.

Part Baseboard	Manufacturer	Manufacturer Part No.
X1,X2,X3,X4	Hirose	FX10A-100S/10-SV

Table 3-1: Baseboard connector types

The connectors on the CM-i.MX31C are of the following type:

Part	Manufacturer	Manufacturer Part No.
X1 – X4	Hirose 4mm height	FX10A-100P/10-SV

Table 3-2: Core Module connector types

Note: The 5mm height version of the FX10A-100P connector (FX10A-100P/10-SV1) is available upon request!

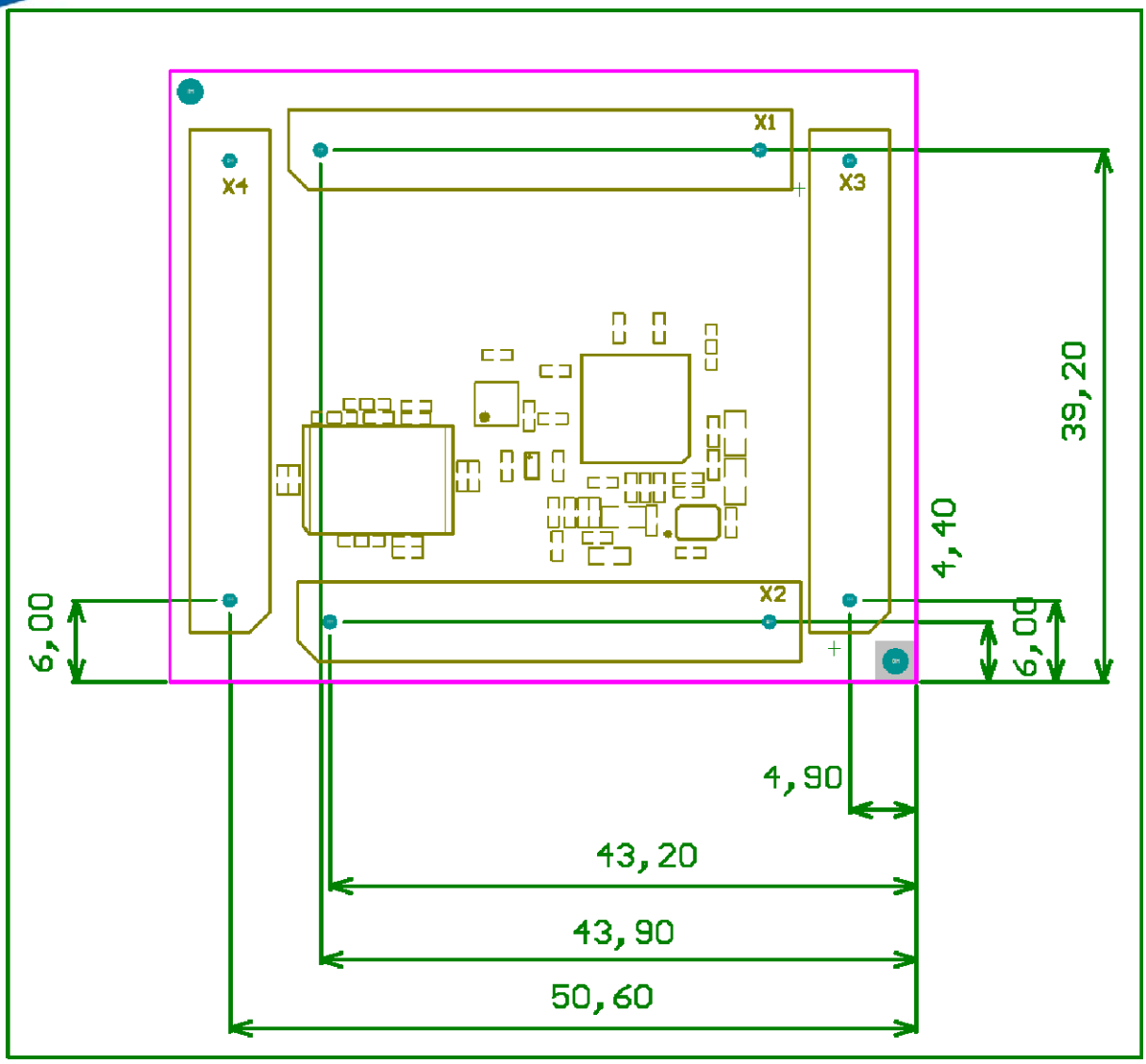

Figure 3-3: FX10A-100P/10-SV connector placement (bottom view)

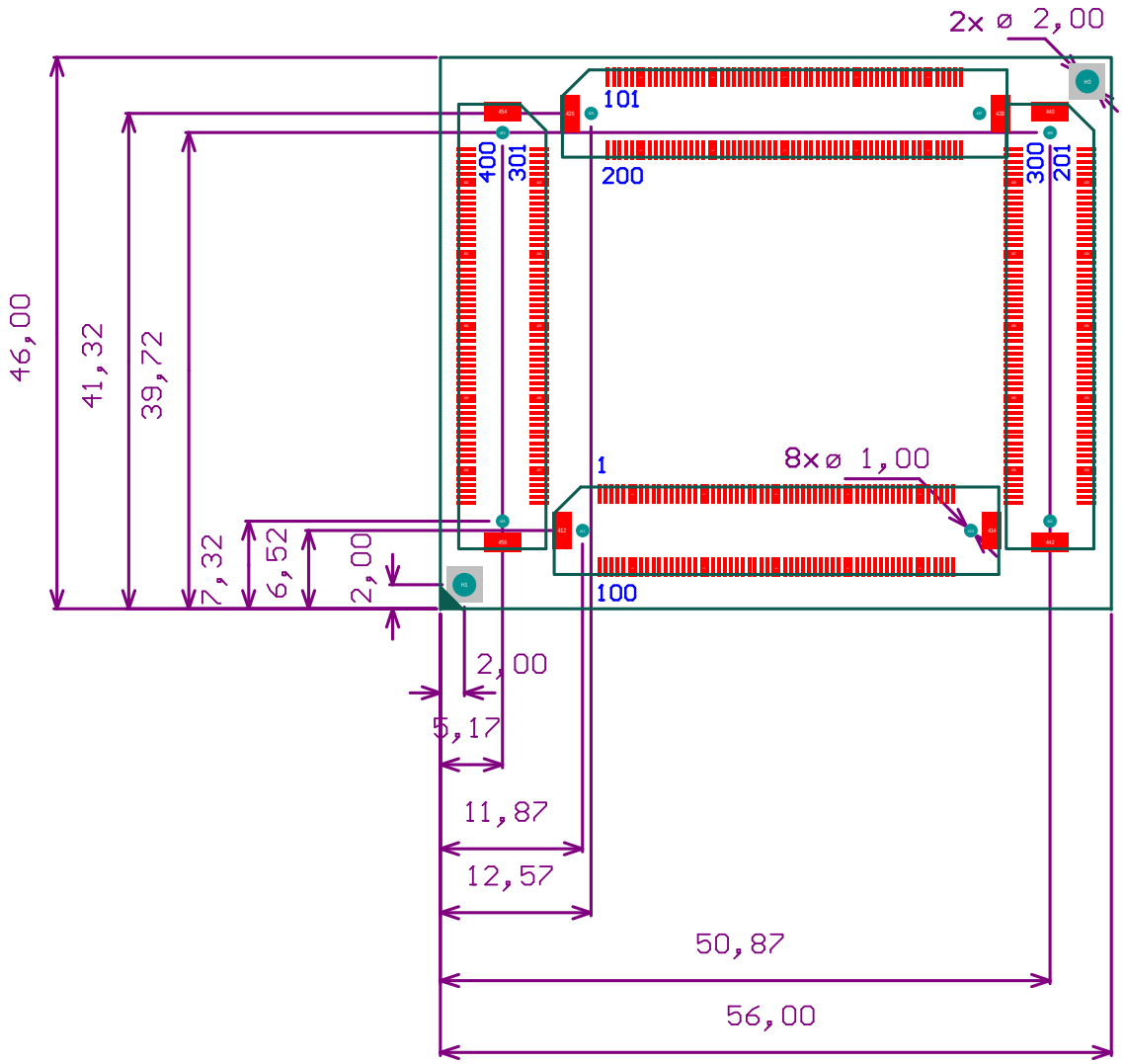

Figure 3-4: Recommended footprint for the Base Board (top view)

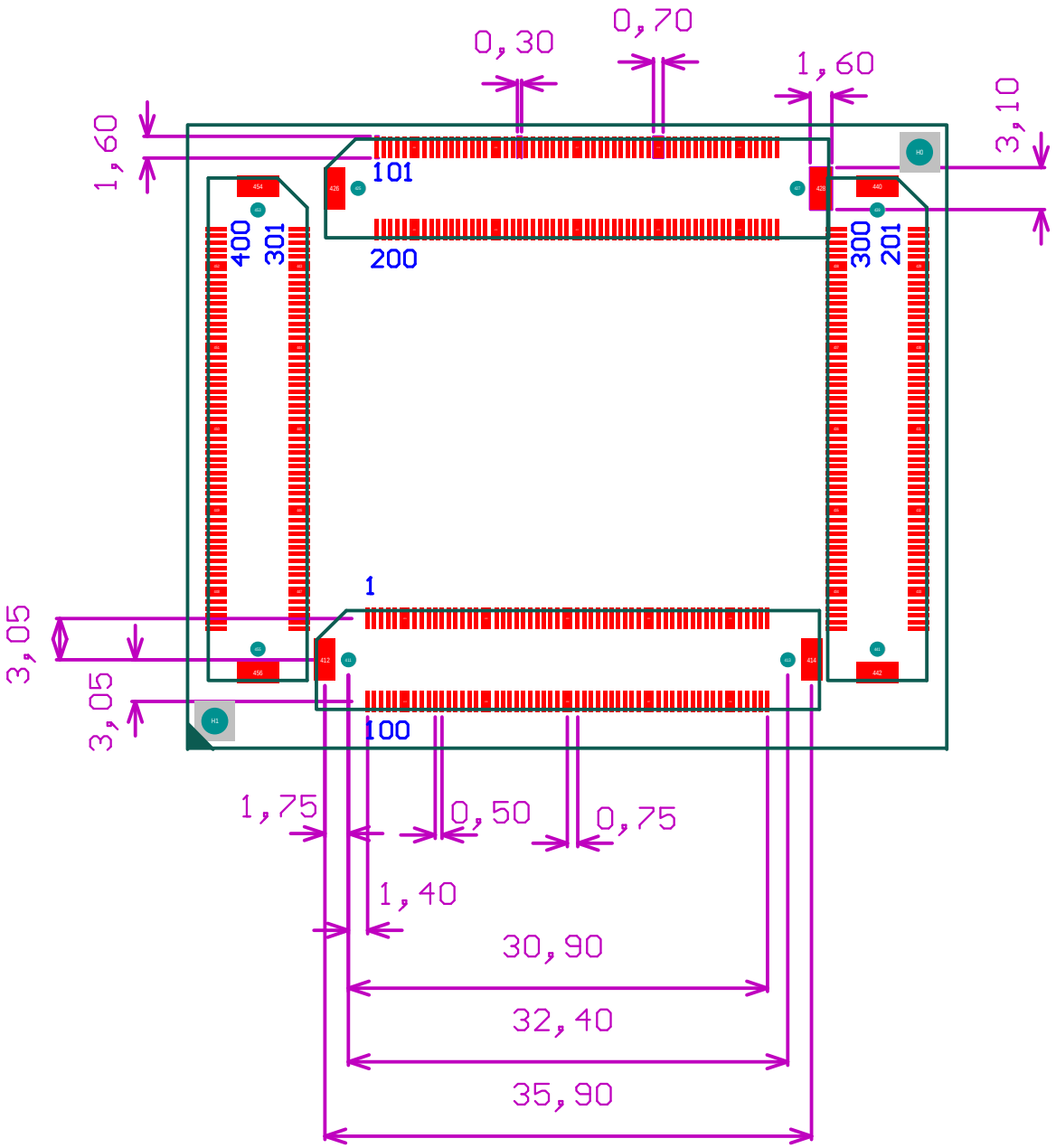

Figure 3-5: Detailed footprint with pad dimensions

4 CM-i.MX31B Ball Grid Array Version (BGA)

4.1 Mechanical Outline

All dimensions are given in millimetres!

The outline of the Core Module can vary between 45mm/55mm and 46mm/56mm.

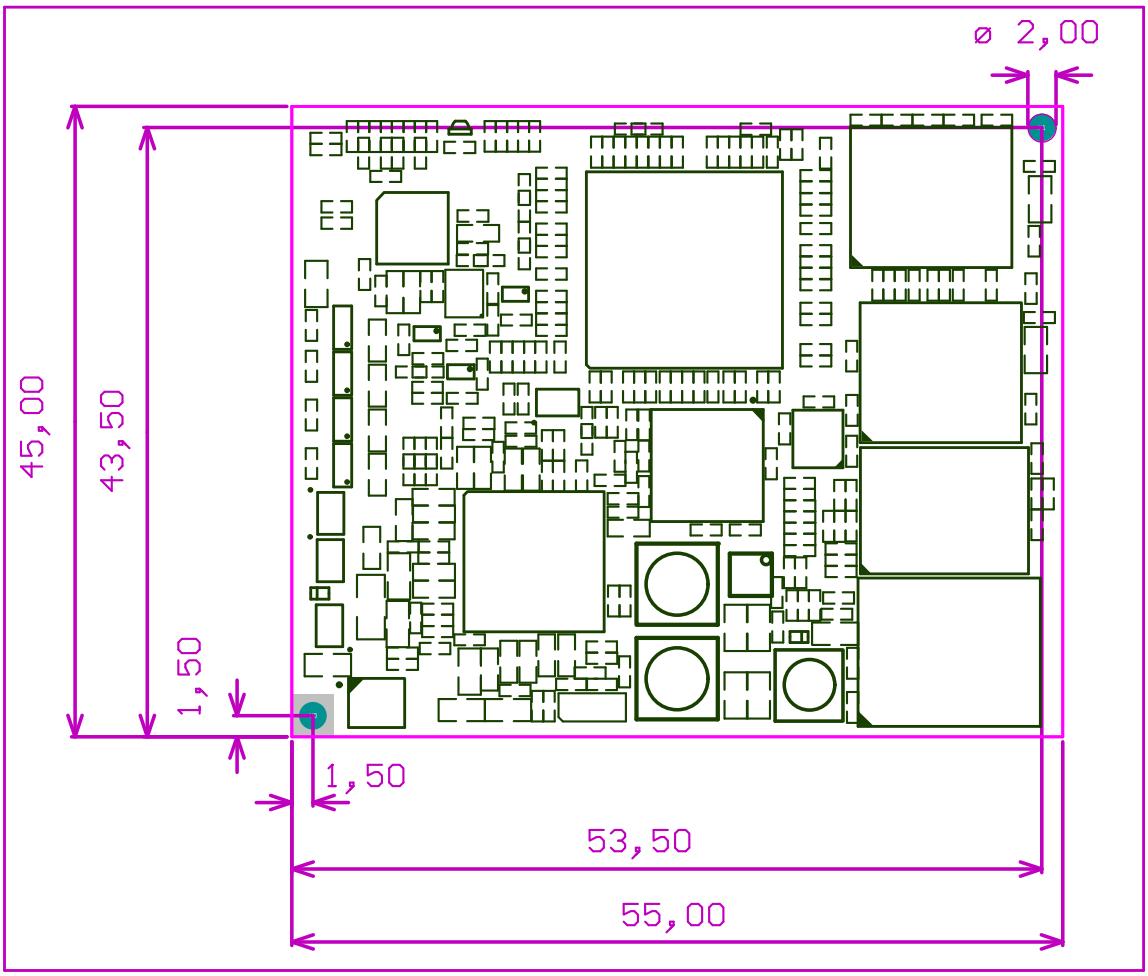

Figure 4-1: Mechanical outline (top view)

The mechanical outline represents a top view, the BGAs (Ball Grids) are placed at the bottom of the Core Module.

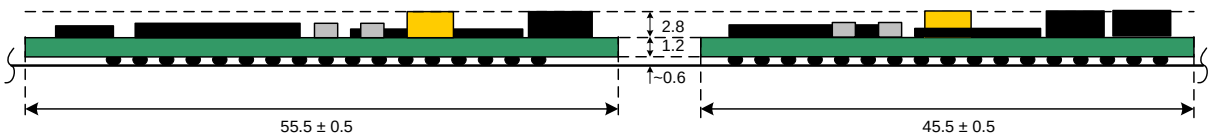

Figure 4-2: Side View with Connector mounted

The total minimum mounting height from the baseboard is 4.6mm.

4.2 Recommended Footprint of BGA Version

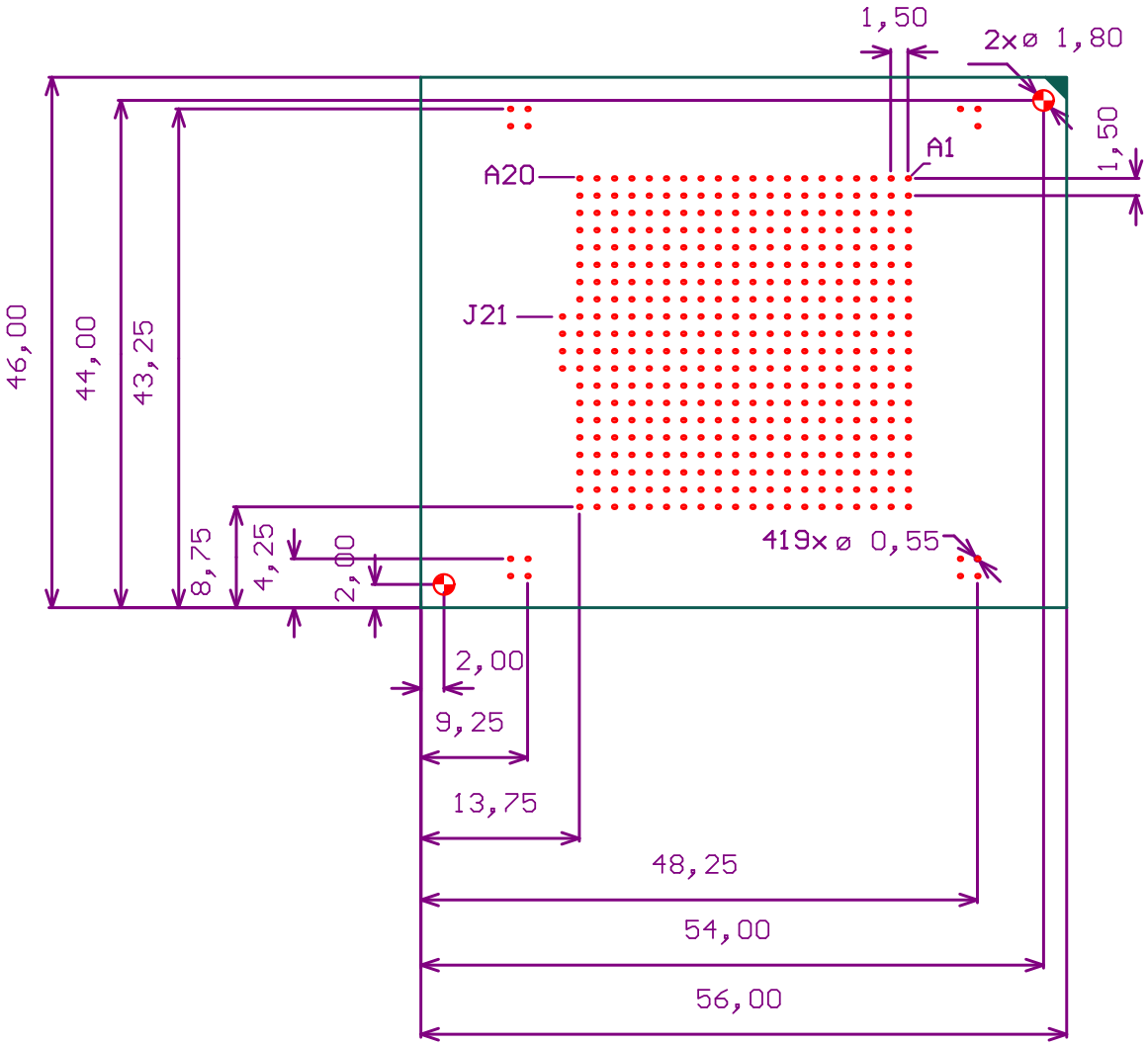

Figure 4-3: BGA footprint for the Core Module (top view)

4.3 BGA Numbering

Note: J21, K21, l21, M21 and X1 to X15 are reserved. Do not connect these pins!

X5	X4																			X2	X1
X7	X6																				X3
		A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
		B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
		C20	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1
		D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
		E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1
		F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1
		G20	G19	G18	G17	G16	G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1
		H20	H19	H18	H17	H16	H15	H14	H13	H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1
J21		J20	J19	J18	J17	J16	J15	J14	J13	J12	J11	J10	J9	J8	J7	J6	J5	J4	J3	J2	J1
K21		K20	K19	K18	K17	K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1
L21		L20	L19	L18	L17	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1
M21		M20	M19	M18	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1
		N20	N19	N18	N17	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
		P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1
		R20	R19	R18	R17	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
		T20	T19	T18	T17	T16	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1
		U20	U19	U18	U17	U16	U15	U14	U13	U12	U11	U10	U9	U8	U7	U6	U5	U4	U3	U2	U1
		V20	V19	V18	V17	V16	V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1
		W20	W19	W18	W17	W16	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1
		Y20	Y19	Y18	Y17	Y16	Y15	Y14	Y13	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
X13	X12																			X9	X8
X15	X14																			X11	X10

Figure 4-4 BGA Numbering (top view)

5 Pin Assignment

Pin assignment for connector and BGA. For BGA numbering, see chapter 4.

5.1.1 Sub Symbol A – USB Group

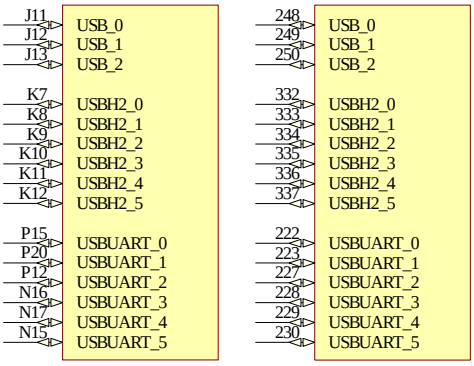

Figure 5-1: Connector Sub-Symbol A

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
J11	248	USB_0	USB	USB_PWR/MAX1_HM_0/MCU1_29	I/O	NVCC5	MCIMX31
J12	249	USB_1	USB	USB_OC/MAX1_HM_1/MCU1_30	I/O	NVCC5	MCIMX31
J13	250	USB_2	USB	USB_BYP/MAX1_HM_2/MCU1_31	I/O	NVCC5	MCIMX31
K7	332	USBH2_0	USB	USBH2_CLK/ATA_INTRQ/UART5_RTS/TD_20	I/O	NVCC10	MCIMX31
K8	333	USBH2_1	USB	USBH2_STP/ATA_DMARQ/UART5_TXD/TD_22	I/O	NVCC10	MCIMX31
K9	334	USBH2_2	USB	USBH2_NXT/ATA_DA0/UART5_CTS/TD_23	I/O	NVCC10	MCIMX31
K10	335	USBH2_3	USB	USBH2_DIR/ATA_DIR/UART5_RXD/TD_21	I/O	NVCC10	MCIMX31
K11	336	USBH2_4	USB	USBH2_D1/ATA_DA2/TRCLK	I/O	NVCC10	MCIMX31
K12	337	USBH2_5	USB	USBH2_D0/ATA_DA1/TRCTL	I/O	NVCC10	MCIMX31
P15	222	USBUART_0	USB	UDATVP	I/O	LV	MC13783
P20	223	USBUART_1	USB	USEOVM	I/O	LV	MC13783
P12	227	USBUART_2	USB	UTXENB	I/O	LV	MC13783
N16	228	USBUART_3	USB	URCVD	I/O	LV	MC13783
N17	229	USBUART_4	USB	URXVM	I/O	LV	MC13783
N15	230	USBUART_5	USB	URXVP	I/O	LV	MC13783

Table 5-1: Connector Sub-Symbol A

5.1.2 Sub Symbol B - IPU Group

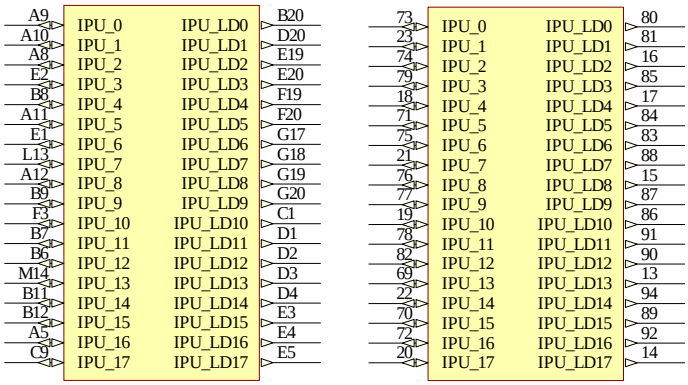

Figure 5-2: Connector Sub-Symbol B

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
A9	73	IPU_0	IPU	SD_D_IO/DB-CS-3/MCU3-21	I/O	NVCC7	MCIMX31
A10	23	IPU_1	IPU	SD_D_I/SD_D_I/SDB_CS_2/ MCU3_20	I/O	NVCC7	MCIMX31
A8	74	IPU_2	IPU	SD_D_CLK/MCU3_22	I/O	NVCC7	MCIMX31
E2	79	IPU_3	IPU	SER_RS/MCU3_22	I/O	NVCC7	MCIMX31
B8	18	IPU_4	IPU	PAR_RS	I/O	NVCC7	MCIMX31
A 11	71	IPU_5	IPU	VSYNC0/SDB_EC_4	I/O	NVCC7	MCIMX31
E1	75	IPU_6	IPU	VSYNC3	I/O	NVCC7	MCIMX31
L13	21	IPU_7	IPU	READ	I/O	NVCC7	MCIMX31
A 12	76	IPU_8	IPU	WRITE	I/O	NVCC7	MCIMX31
B9	77	IPU_9	IPU	CONTRAST	I/O	NVCC7	MCIMX31
F3	19	IPU_10	IPU	D3_CLS	I/O	NVCC7	MCIMX31
B7	78	IPU_11	IPU	D3_REV	I/O	NVCC7	MCIMX31
B6	82	IPU_12	IPU	D3_SPL	I/O	NVCC7	MCIMX31
M14	69	IPU_13	IPU	DRDY0/SDB_CS_1	I/O	NVCC7	MCIMX31
B11	22	IPU_14	IPU	FPSHIFT/DISPB_BCLK/SDB _CS_0	I/O	NVCC7	MCIMX31
B12	70	IPU_15	IPU	HSYNC/SDB_EC_5	I/O	NVCC7	MCIMX31
A 5	72	IPU_16	IPU	LCS0/DISPB_BCLK/MCU3_2 3	I/O	NVCC7	MCIMX31
C9	20	IPU_17	IPU	LSC1/MCU3_24	I/O	NVCC7	MCIMX31
B20	80	IPU_LD0	IPU_LD	LD0/SDB_PC_0	O	NVCC7	MCIMX31
D20	81	IPU_LD1	IPU_LD	LD1/SDB_PC_1	O	NVCC7	MCIMX31
E19	16	IPU_LD2	IPU_LD	LD2/SDB_PC_2	O	NVCC7	MCIMX31
E20	85	IPU_LD3	IPU_LD	LD3/SDB_PC_3	O	NVCC7	MCIMX31
F19	17	IPU_LD4	IPU_LD	LD4/SDB_PC_4	O	NVCC7	MCIMX31
F20	84	IPU_LD5	IPU_LD	LD5/SDB_PC_5	O	NVCC7	MCIMX31
G17	83	IPU_LD6	IPU_LD	LD6/SDB_PC_6	O	NVCC7	MCIMX31
G18	88	IPU_LD7	IPU_LD	LD7/SDB_PC_7	O	NVCC7	MCIMX31
G19	15	IPU_LD8	IPU_LD	LD8/SDB_PC_8	O	NVCC7	MCIMX31

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
G20	87	IPU_LD9	IPU_LD	LD9/SDB_PC_9	O	NVCC7	MCIMX31
C1	86	IPU_LD10	IPU_LD	LD10/SDB_PC_10	O	NVCC7	MCIMX31
D1	91	IPU_LD11	IPU_LD	LD11/SDB_PC_11	O	NVCC7	MCIMX31
D2	90	IPU_LD12	IPU_LD	LD12/SDB_PC_12	O	NVCC7	MCIMX31
D3	13	IPU_LD13	IPU_LD	LD13/SDB_PC_13	O	NVCC7	MCIMX31
D4	94	IPU_LD14	IPU_LD	LD14/SDB_EC_0	O	NVCC7	MCIMX31
E3	89	IPU_LD15	IPU_LD	LD15/SDB_EC_1	O	NVCC7	MCIMX31
E4	92	IPU_LD16	IPU_LD	LD16/SDB_EC_2	O	NVCC7	MCIMX31
E5	14	IPU_LD17	IPU_LD	LD17/SDB_EC_3	O	NVCC7	MCIMX31

Table 5-2: Connector Sub-Symbol B

5.1.3 Sub Symbol C - UART Group

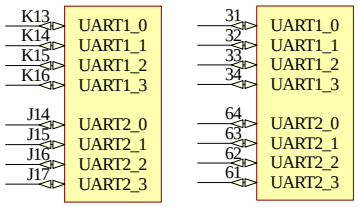

Figure 5-3: Connector Sub-Symbol C

Ball	Pin	Pin	Group	Description	Signal type	Power Domain	Chip
K13	31	UART1_0	UART	UART1_TXD/TKC/USBOTG_D1/PP4_CLK/RI_DCE1/MCU2_5	I/O	NVCC8	MCIMX31
K14	32	UART1_1	UART	UART1_RXD/TRSTB/USBOTG_D4/PP4_TXDAT/DSR_DCE1/MCU2_4	I/O	NVCC8	MCIMX31
K15	33	UART1_2	UART	UART1_RTS/PP4_FS/DCD_DCE1/MCU2_6	I/O	NVCC8	MCIMX31
K16	34	UART1_3	UART	UART1_CTS/DE_B/MCU2_7	I/O	NVCC8	MCIMX31
J14	64	UART2_0	UART	UART2_TXD/MCU1_28	I/O	NVCC8	MCIMX31
J15	63	UART2_1	UART	UART2_RXD/MCU1_27	I/O	NVCC8	MCIMX31
J16	62	UART2_2	UART	UART2_RTS	I/O	NVCC8	MCIMX31
J17	61	UART2_3	UART	UART2_CTS	I/O	NVCC8	MCIMX31

Table 5-3: Connector Sub-Symbol C

5.1.4 Sub Symbol D - JTAG, RESET, CLK

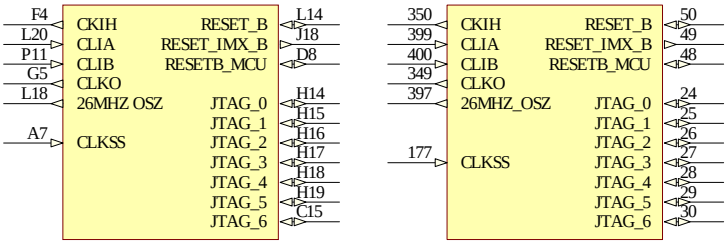

Figure 5-4: Connector Sub-Symbol C

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
F4	350	CKIH	JTAG	CKIH	O	NVCC1	MCIMX31
L20	399	CLIA	JTAG	CLIA	I	LV	MCIMX31
P11	400	CLIB	JTAG	CLIB	I	LV	MCIMX31
G5	349	CLKO	JTAG	CLKO	O	NVCC1	MCIMX31
H14	24	JTAG_0	JTAG	DE_B	I/O	NVCC6	MCIMX31
H15	25	JTAG_1	JTAG	TCK	I/O	NVCC6	MCIMX31
H16	26	JTAG_2	JTAG	TDI	I/O	NVCC6	MCIMX31
H17	27	JTAG_3	JTAG	TDO	I/O	NVCC6	MCIMX31
H18	28	JTAG_4	JTAG	TMS	I/O	NVCC6	MCIMX31
H19	29	JTAG_5	JTAG	TRSTB	I/O	NVCC6	MCIMX31
C15	30	JTAG_6	JTAG	RTCK	I/O	NVCC6	MCIMX31
L14	50	RESET_B	JTAG	POR_B (for JTAG)	I/O	NVCC1	MCIMX31
J18	49	RESET_IMX_B	JTAG	Reset output for application	O	NVCC1	MCIMX31
D8	48	RESETB_MCU	JTAG	Reset for MCU	I/O		MCIMX31
A7	177	CLKSS	JTAG	Clock Select (between 32kHz and 26MHz)	I		MCIMX31
L18	397	26MHZ OSZ	JTAG	26MHz output	O		MCIMX31

Table 5-4: Connector Sub-Symbol D

5.1.5 Sub Symbol E - PCMCIA, MMC, I2C

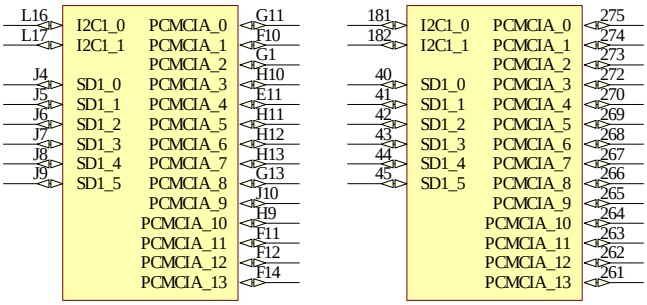

Figure 5-5: Connector Sub-Symbol E

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
L16	181	I2C1_0	MMC	I2C1_CLK/ATA_D14	I/O	NVCC4	MCIMX31
L17	182	I2C1_1	MMC	I2C1_DAT/ATA_D15	I/O	NVCC4	MCIMX31
G11	275	PCMCIA0	MMC	PC_BVD1/USBH2_D3/UART5_RXD	I/O	NVCC3	MCIMX31
F10	274	PCMCIA1	MMC	PC_BVD2/USBH2_D4/UART5_TXD	I/O	NVCC3	MCIMX31
G1	273	PCMCIA2	MMC	PC_CD1_B/SD2_CMD/MSHC2_BS	I/O	NVCC3	MCIMX31
H10	272	PCMCIA3	MMC	PC_CD2_B/SD2_CLK/MSHC2_BS	I/O	NVCC3	MCIMX31
E11	270	PCMCIA4	MMC	PC_POE	I/O	NVCC3	MCIMX31
H11	269	PCMCIA5	MMC	PC_PWRON/SD_D3/MSHC2_D2	I/O	NVCC3	MCIMX31
H12	268	PCMCIA6	MMC	PC_READY/SD2_D1/MSHC2_D1	I/O	NVCC3	MCIMX31
H13	267	PCMCIA7	MMC	PC_RST/USBH2_D5/UART5_CTS	I/O	NVCC3	MCIMX31
G13	266	PCMCIA8	MMC	PC_RW_B/USBH2_D7	I/O	NVCC3	MCIMX31
J10	265	PCMCIA9	MMC	PC_VS1/SD2_D2/MSHC2_D3	I/O	NVCC3	MCIMX31
H9	264	PCMCIA10	MMC	PC_VS2/USBH2_D2/UART5_RTS	I/O	NVCC3	MCIMX31
F11	263	PCMCIA11	MMC	PC_WAIT_B/SD2_D0/MSHC2_SDIO_D0	I/O	NVCC3	MCIMX31
F12	262	PCMCIA12	MMC	IOIS16/USBH2_D6	I/O	NVCC3	MCIMX31
F14	261	PCMCIA13	MMC	PWMO/ATA_IORDY/PC_SPKOUT/MCU1_9	I/O	NVCC3	MCIMX31
J4	40	SD1_0	MMC	SDI_CLK/MSHC1_BS/TD_1/MCU2_27	I/O	NVCC3	MCIMX31
J5	41	SD1_1	MMC	SDI_CMD/MSHC1_SCLK/TD_0/MCU2_26	I/O	NVCC3	MCIMX31
J6	42	SD1_2	MMC	SD1_D3/MSHC1_D3/CTI_TIN_1_7/TD_5/MCU2_31	I/O	NVCC3	MCIMX31
J7	43	SD1_3	MMC	SD1_D2/MSHC1_D2/TD_4/MCU2_30	I/O	NVCC3	MCIMX31
J8	44	SD1_4	MMC	SD1_D1/MSHC1_D1/TD_3/MCU2_29	I/O	NVCC3	MCIMX31
J9	45	SD1_5	MMC	SD1_D0/MSHC1_SDIO-D0/TD_2/MCU2_28	I/O	NVCC3	MCIMX31

Table 5-5: Connector Sub-Symbol E

5.1.6 Sub Symbol F - MCU1 Group

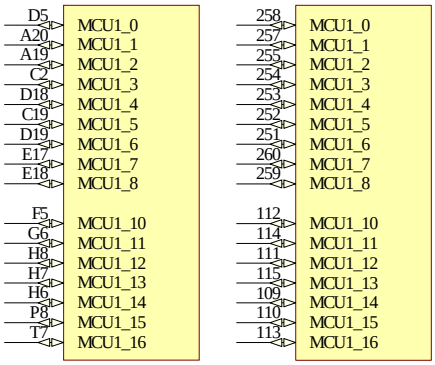

Figure 5-6: Connector Sub-Symbol F

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
D5	258	MCU1_0	MCU1	GPIO1_0/EXTDMA_0/MCU1_0	I/O	NVCC1	MCIMX31
A20	257	MCU1_1	MCU1	GPIO1_1/EXTDMA_0/MCU1_1	I/O	NVCC1	MCIMX31
A19	255	MCU1_2	MCU1	GPIO1_2/EXTDMA_0/MCU1_2	I/O	NVCC1	MCIMX31
C2	254	MCU1_3	MCU1	GPIO1_3/MCU1_3	I/O	NVCC1	MCIMX31
D18	253	MCU1_4	MCU1	GPIO1_4/USBH1_SUSPEND/MCU1_4	I/O	NVCC1	MCIMX31
C19	252	MCU1_5	MCU1	GPIO1_5/MCU1_5	I/O	NVCC1	MCIMX31
D19	251	MCU1_6	MCU1	GPIO1_6/TMPR_DTCT/MCU1_6	I/O	NVCC1	MCIMX31
E17	260	MCU1_7	MCU1	CAPTURE/ATA_D14/CMP2/MCU1_7	I/O	NVCC1	MCIMX31
E18	259	MCU1_8	MCU1	COMPARE/ATA_D15/CAP2/CMP3/MCU1_8	I/O	NVCC1	MCIMX31
F5	112	MCU1_10	MCU1	NFWE_B/ATA_INTRQ/USBH2_D2/TD_0/MCU1_10	I/O	NVCC10	MCIMX31
G6	114	MCU1_11	MCU1	NFRE_B/ATA_D8/ATA_DIR/USBH2_D3/TD_1MCU1_11	I/O	NVCC10	MCIMX31
H8	111	MCU1_12	MCU1	NFALE/ATA_D9/ATA_DMARQ/USBH2_D4/TD_2/MCU1_12	I/O	NVCC10	MCIMX31
H7	115	MCU1_13	MCU1	NFCLE/ATA_D10/ATA_DA0/USBH2_D5/TD_3/MCU1_13	I/O	NVCC10	MCIMX31
H6	109	MCU1_14	MCU1	NFWP_B/ATA_D11/ATA_DA1/NFWP_B/USBH2_D6/TD_4/MCU1_14	I/O	NVCC10	MCIMX31
P8	110	MCU1_15	MCU1	NFCE/ATA_DATA12/ATA_DA2/TRACEDATA_6/MCU1_15	I/O	NVCC10	MCIMX31
T7	113	MCU1_16	MCU1	NFRB/ATA_DATA13/TRACEDATA_6/MCU1_16	I/O	NVCC10	MCIMX31

Table 5-6: Connector Sub-Symbol F

5.1.7 Sub Symbol G – MCU2 Group

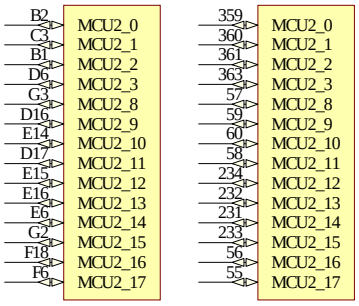

Figure 5-7: Connector Sub-Symbol G

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
B2	359	MCU2_0	MCU2	SVEN0/CTI_TIN_1_6/MCU2_0	I/O	NVCC9	MCIMX31
C3	360	MCU2_1	MCU2	STX0/CTI_TIN_1_5/MCU2_1	I/O	NVCC9	MCIMX31
B1	361	MCU2_2	MCU2	SRX0/MCU2_2	I/O	NVCC9	MCIMX31
D6	363	MCU2_3	MCU2	SIMPD0/MCU2_3	I/O	NVCC9	MCIMX31
G3	57	MCU2_8	MCU2	DTR_DCE1/TMS/PP4_RXDAT/MCU2_8	I/O	NVCC8	MCIMX31
D16	59	MCU2_9	MCU2	DSR_DCE1/TD0/USBOTG_D4/CSPI1_SCLK/TXD1/DSR_DCE2/MCU2_9	I/O	NVCC8	MCIMX31
E14	60	MCU2_10	MCU2	RI_DCE1/TDI/USBOTG_D3/CSPI1_RDY/RXD1/RI_DCE2/MCU2_10	I/O	NVCC8	MCIMX31
D17	58	MCU2_11	MCU2	DCD_DCE1//RESET_IN/USBOTG_D5/CSPI1_SS3/RTS1/DCD_DCE2/USB_PWR/MCU2_11	I/O	NVCC8	MCIMX31
E15	234	MCU2_12	MCU2	DTR_DTE1/CSPI1_MOSI/DTR_DTE2/I2C_EVTNBUS_16/MCU2_12	I/O	NVCC8	MCIMX31
E16	232	MCU2_13	MCU2	DSR_DTE1/CSPI1_MISO/DSR_DTE2/MCU2_13	I/O	NVCC8	MCIMX31
E6	231	MCU2_14	MCU2	RI_DTE/CSPI1_SS0/RI_DTE2/I2C2_SCL/EVNTBUS_18/MCU2_14	I/O	NVCC8	MCIMX31
G2	233	MCU2_15	MCU2	DCD_DTE1/CSPI1_SS1/DCD_DTE2/I2C2_SDA/MCU2_15	I/O	NVCC8	MCIMX31
F18	56	MCU2_16	MCU2	DTR_DCE2/CSPI1_SS2/MCU2_16	I/O	NVCC8	MCIMX31
F6	55	MCU2_17	MCU2	BATT_LINE	I/O	NVCC5	MCIMX31

Table 5-7: Connector Sub-Symbol G

5.1.8 Sub Symbol H – MCU3 Group

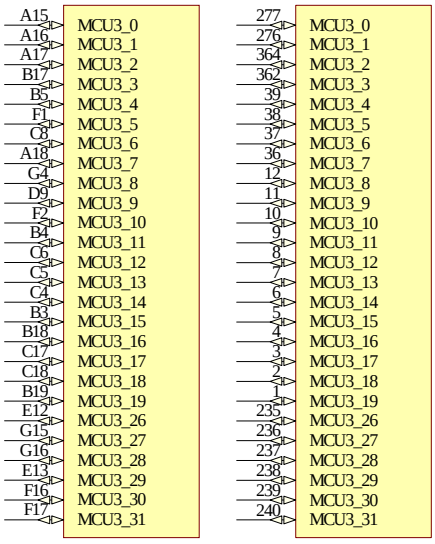

Figure 5-8: Connector Sub-Symbol H

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
A15	277	MCU3_0	MCU3	GPIO3_1/UPLL_BYP_CLK/MCU3_0	I/O	NVCC4	MCIMX31
A16	276	MCU3_1	MCU3	GPIO3_0/SPLL_BYP_CLK/MCU3_1	I/O	NVCC4	MCIMX31
A17	364	MCU3_2	MCU3	SCLK0/CTI_TIN_1_4/DISPB_D2_CS/MCU3_2	I/O	NVCC9	MCIMX31
B17	362	MCU3_3	MCU3	SRST0/DISPB_D12_VSYNC/MCU3_3	I/O	NVCC9	MCIMX31
B5	39	MCU3_4	MCU3	CSI_D4/CTI_TOUT_1_2/MCU3_4	I/O	NVCC4	MCIMX31
F1	38	MCU3_5	MCU3	CSI_D5/CTI_TOUT_1_3/MCU3_5	I/O	NVCC4	MCIMX31
C8	37	MCU3_6	MCU3	CSI_D6/ATA_D0/CTI_TOUT_1_4/MCU3_6	I/O	NVCC4	MCIMX31
A18	36	MCU3_7	MCU3	CSI_D7/ATA_D1/CTI_TOUT_1_5/MCU3_7	I/O	NVCC4	MCIMX31
G4	12	MCU3_8	MCU3	CSI_D8/ATA_D2/MCU3_8	I/O	NVCC4	MCIMX31
D9	11	MCU3_9	MCU3	CSI_D9/ATA_D3/MCU3_9	I/O	NVCC4	MCIMX31
F2	10	MCU3_10	MCU3	CSI_D10/ATA_D4/MCU3_10	I/O	NVCC4	MCIMX31
B4	9	MCU3_11	MCU3	CSI_D11/ATA_D5/MCU3_11	I/O	NVCC4	MCIMX31
C6	8	MCU3_12	MCU3	CSI_D12/ATA_D6/MCU3_12	I/O	NVCC4	MCIMX31
C5	7	MCU3_13	MCU3	CSI_D13/ATA_D7/MCU3_13	I/O	NVCC4	MCIMX31
C4	6	MCU3_14	MCU3	CSI_D14/ATA_D8/MCU3_14	I/O	NVCC4	MCIMX31
B3	5	MCU3_15	MCU3	CSI_D15/ATA_D9/MCU3_15	I/O	NVCC4	MCIMX3

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
							1
B18	4	MCU3_16	MCU3	CSI_VSYNC/ATA_D11/MCU3_17	I/O	NVCC4	MCIMX31
C17	3	MCU3_17	MCU3	CSI_MCLK/ATA_D10/MCU3_16	I/O	NVCC4	MCIMX31
C18	2	MCU3_18	MCU3	CSI_HSYNC/ATA_D12/MCU3_18	I/O	NVCC4	MCIMX31
B19	1	MCU3_19	MCU3	CSI_PIXCLK/ATA_D13/MCU3_19	I/O	NVCC4	MCIMX31
E12	235	MCU3_26	MCU3	ATA_CS0/UART4_RXD/CSI_D0/SD_D_CLK/TD_6/MCU3_26	I/O	NVCC3	MCIMX31
G15	236	MCU3_27	MCU3	ATA_CS1/UART4_RTS/CSI_D1/LCS1/TD_7/MCU3_27	I/O	NVCC3	MCIMX31
G16	237	MCU3_28	MCU3	ATA_DIOR/UART4_TXD/CSI_D2/SER_RS/TRCTL/MCU3_28	I/O	NVCC3	MCIMX31
E13	238	MCU3_29	MCU3	ATA_DIOW/UART4_CTS/CSI_D3/TRCLK/MCU3_29	I/O	NVCC3	MCIMX31
F16	239	MCU3_30	MCU3	ATA_DMACK/SD_D_O/MCU3_30	I/O	NVCC3	MCIMX31
F17	240	MCU3_31	MCU3	ATA_RESET_B/SD_D/MCU3_31	I/O	NVCC3	MCIMX31

Table 5-8: Connector Sub-Symbol H

5.1.9 Sub Symbol I – Data & Address Bus Group

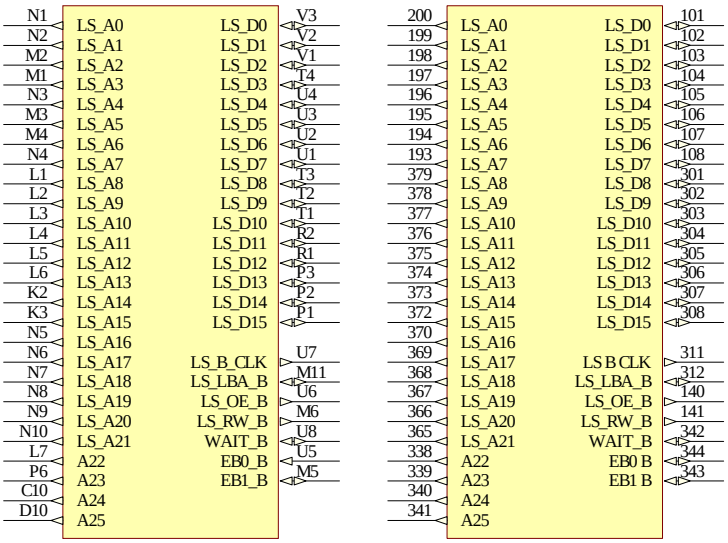

Figure 5-9: Connector Sub-Symbol I

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
N1	200	LS_A0	EMI		O	3V3	MCIMX31
N2	199	LS_A1	EMI		O	3V3	MCIMX31
M2	198	LS_A2	EMI		O	3V3	MCIMX31
M1	197	LS_A3	EMI		O	3V3	MCIMX31

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
N3	196	LS_A4	EMI		O	3V3	MCIMX31
M3	195	LS_A5	EMI		O	3V3	MCIMX31
M4	194	LS_A6	EMI		O	3V3	MCIMX31
N4	193	LS_A7	EMI		O	3V3	MCIMX31
L1	379	LS_A8	EMI		O	3V3	MCIMX31
L2	378	LS_A9	EMI		O	3V3	MCIMX31
L3	377	LS_A10	EMI		O	3V3	MCIMX31
L4	376	LS_A11	EMI		O	3V3	MCIMX31
L5	375	LS_A12	EMI		O	3V3	MCIMX31
L6	374	LS_A13	EMI		O	3V3	MCIMX31
K2	373	LS_A14	EMI		O	3V3	MCIMX31
K3	372	LS_A15	EMI		O	3V3	MCIMX31
N5	370	LS_A16	EMI		O	3V3	MCIMX31
N6	369	LS_A17	EMI		O	3V3	MCIMX31
N7	368	LS_A18	EMI		O	3V3	MCIMX31
N8	367	LS_A19	EMI		O	3V3	MCIMX31
N9	366	LS_A20	EMI		O	3V3	MCIMX31
N10	365	LS_A21	EMI		O	3V3	MCIMX31
L7	338	A22	EMI		O	P_SW2	MCIMX31
P6	339	A23	EMI		O	P_SW2	MCIMX31
C10	340	A24	EMI		O	P_SW2	MCIMX31
D10	341	A25	EMI		O	P_SW2	MCIMX31
U7	311	LS_B_CLK	EMI		O	3V3	MCIMX31
V3	101	LS_D0	EMI		I/O	3V3	MCIMX31
V2	102	LS_D1	EMI		I/O	3V3	MCIMX31
V1	103	LS_D2	EMI		I/O	3V3	MCIMX31
T4	104	LS_D3	EMI		I/O	3V3	MCIMX31
U4	105	LS_D4	EMI		I/O	3V3	MCIMX31
U3	106	LS_D5	EMI		I/O	3V3	MCIMX31
U2	107	LS_D6	EMI		I/O	3V3	MCIMX31
U1	108	LS_D7	EMI		I/O	3V3	MCIMX31
T3	301	LS_D8	EMI		I/O	3V3	MCIMX31
T2	302	LS_D9	EMI		I/O	3V3	MCIMX31
T1	303	LS_D10	EMI		I/O	3V3	MCIMX31
R2	304	LS_D11	EMI		I/O	3V3	MCIMX31
R1	305	LS_D12	EMI		I/O	3V3	MCIMX31
P3	306	LS_D13	EMI		I/O	3V3	MCIMX31
P2	307	LS_D14	EMI		I/O	3V3	MCIMX31
P1	308	LS_D15	EMI		I/O	3V3	MCIMX31
U5	344	EB0_B	EMI		I/O	P_SW2	MCIMX31
M5	343	EB1_B	EMI		I/O	P_SW2	MCIMX31
M11	312	LS_LBA_B	EMI		I/O	3V3	MCIMX31
U6	140	LS_OE_B	EMI		O	3V3	MCIMX31
U8	342	WAIT B	EMI		I/O	P_SW2	MCIMX31
M6	141	LS_RW_B	EMI		O	3V3	MCIMX31

Table 5-9: Connector Sub-Symbol I

5.1.10 Sub Symbol J – Keypad Group

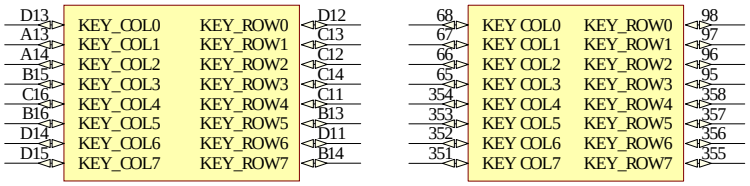

Figure 5-10: Connector Sub-Symbol J

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
D13	68	KEY_COL0	KEY_COL	KEY_COL0	I/O	NVCC6	MCIMX31
A13	67	KEY_COL1	KEY_COL	KEY_COL1	I/O	NVCC6	MCIMX31
A14	66	KEY_COL2	KEY_COL	KEY_COL2	I/O	NVCC6	MCIMX31
B15	65	KEY_COL3	KEY_COL	KEY_COL3/TD3	I/O	NVCC6	MCIMX31
C16	354	KEY_COL4	KEY_COL	KEY_COL4/ATA_DMARQ/TD_4/MCU2_22	I/O	NVCC6	MCIMX31
B16	353	KEY_COL5	KEY_COL	KEY_COL5/ATA_DA0/TD_5/MCU2_23	I/O	NVCC6	MCIMX31
D14	352	KEY_COL6	KEY_COL	KEY_COL6/ATA_DA1/TD_6/MCU2_24	I/O	NVCC6	MCIMX31
D15	351	KEY_COL7	KEY_COL	KEY_COL7/ATA_DA2/TD_7/MCU2_25	I/O	NVCC6	MCIMX31
D12	98	KEY_ROW0	KEY_ROW	KEY_ROW0	I/O	NVCC6	MCIMX31
C13	97	KEY_ROW1	KEY_ROW	KEY_ROW1	I/O	NVCC6	MCIMX31
C12	96	KEY_ROW2	KEY_ROW	KEY_ROW2	I/O	NVCC6	MCIMX31
C14	95	KEY_ROW3	KEY_ROW	KEY_ROW3/TRCTL	I/O	NVCC6	MCIMX31
C11	358	KEY_ROW4	KEY_ROW	KEY_ROW4/TRCLK/MCU2_18	I/O	NVCC6	MCIMX31
B13	357	KEY_ROW5	KEY_ROW	KEY_ROW5/TD_0/MCU2_19	I/O	NVCC6	MCIMX31
D11	356	KEY_ROW6	KEY_ROW	KEY_ROW6/ATA_INTRQ/TD_1/MCU2_20	I/O	NVCC6	MCIMX31
B14	355	KEY_ROW7	KEY_ROW	KEY_ROW7/ATA_BUF_EN/TD_2/MCU2_21	I/O	NVCC6	MCIMX31

Table 5-10: Connector Sub-Symbol H

5.1.11 Sub Symbol K – Analog IN/OUT Group

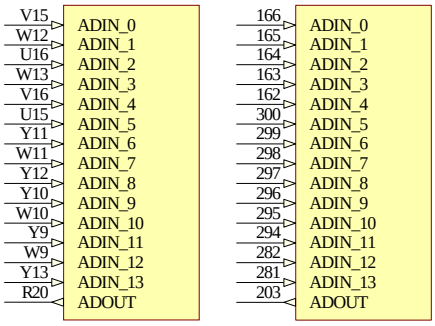

Figure 5-11: Connector Sub-Symbol K

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
V15	166	ADIN0	ADC	ADTRIG	I	-	MC13783
W12	165	ADIN1	ADC	TSX1	I	-	MC13783
U16	164	ADIN2	ADC	TSX2	I	-	MC13783
W13	163	ADIN3	ADC	TSY1	I	-	MC13783
V16	162	ADIN4	ADC	TSY2	I	-	MC13783
U15	300	ADIN5	ADC	ADIN5	I	-	MC13783
Y11	299	ADIN6	ADC	ADIN6	I	-	MC13783
W11	298	ADIN7	ADC	ADIN7	I	-	MC13783
Y12	297	ADIN8	ADC	ADIN8	I	-	MC13783
Y10	296	ADIN9	ADC	ADIN9	I	-	MC13783
W10	295	ADIN10	ADC	ADIN10	I	-	MC13783
Y9	294	ADIN11	ADC	ADIN11	I	-	MC13783
W9	282	ADIN12	ADC	ADIN12	I	-	MC13783
Y13	281	ADIN13	ADC	ADIN13	I	-	MC13783
R20	203	ADOUT	ADC	ADOUT	O	-	MC13783

Table 5-11: Connector Sub-Symbol K

5.1.12 Sub Symbol L – Lighting

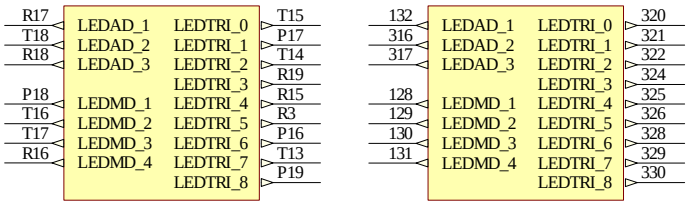

Figure 5-12: Connector Sub-Symbol L

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
R17	132	LEDAD1	LED_AD	LEDAD1	O	-	MC13783
T18	316	LEDAD2	LED_AD	LEDAD2	O	-	MC13783
R18	317	LEDAD3	LED_AD	LEDKP	O	-	MC13783
P18	128	LEDMD1	LED_MD	LEDMD1	O	-	MC13783
T16	129	LEDMD2	LED_MD	LEDMD2	O	-	MC13783

T17	130	LEDMD3	LED_MD	LEDMD3	O	-	MC13783
R16	131	LEDMD4	LED_MD	LEDMD4	O	-	MC13783
T15	320	LEDTRI0	LED_TRI	LEDG1	O	-	MC13783
P17	321	LEDTRI1	LED_TRI	LEDR1	O	-	MC13783
T14	322	LEDTRI2	LED_TRI	LEDB1	O	-	MC13783
R19	324	LEDTRI3	LED_TRI	LEDG2	O	-	MC13783
R15	325	LEDTRI4	LED_TRI	LEDR2	O	-	MC13783
R3	326	LEDTRI5	LED_TRI	LEDB2	O	-	MC13783
P16	328	LEDTRI6	LED_TRI	LEDG3	O	-	MC13783
T13	329	LEDTRI7	LED_TRI	LEDR3	O	-	MC13783
P19	330	LEDTRI8	LED_TRI	LEDB3	O	-	MC13783

Table 5-12: Connector Sub-Symbol L

5.1.13 Sub Symbol M – Audio Codec Interfaces

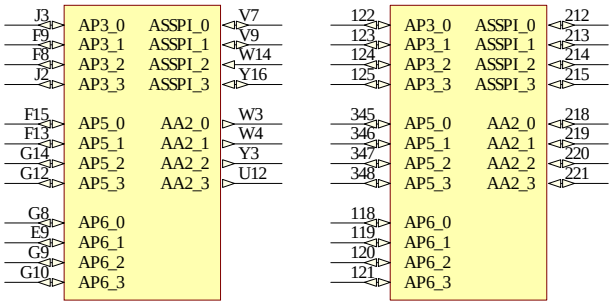

Figure 5-13: Connector Sub-Symbol M

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
W3	218	AA2_0	AP	TX2	I/O	LV	MC13783
W4	219	AA2_1	AP	FS2	I/O	LV	MC13783
Y3	220	AA2_2	AP	BCL2	I/O	LV	MC13783
U12	221	AA2_3	AP	RX2	I/O	LV	MC13783
J3	122	AP3_0	AP	STXD3/ATA_D8/USBH2_D3/TD_8/EMI_DBG1/MCU1_17	I/O	NVCC10	MCIMX31
F9	123	AP3_1	AP	STXD3/ATA_D7/USBH2_D2/TD_7/EMI_DBG0/MCU1_18	I/O	NVCC10	MCIMX31
F8	124	AP3_2	AP	SFS3/ATA_D10/USBH2_D5/TD_10/EMI_DBG3	I/O	NVCC10	MCIMX31
J2	125	AP3_3	AP	SKC3/ATA_D9/USBH2_D4/TD_9/EMI_DBG2	I/O	NVCC10	MCIMX31
F15	345	AP5_0	AP	STXD5/ARM_CRASID3/MCU1_21	I/O	NVCC5	MCIMX31
F13	346	AP5_1	AP	SRXD5/ARM_CRASID4/MCU1_23	I/O	NVCC5	MCIMX31
G14	347	AP5_2	AP	SFS5/ARM_CRASID6	I/O	NVCC5	MCIMX31
G12	348	AP5_3	AP	SCK5/ARM_CRASID5	I/O	NVCC5	MCIMX31
G8	118	AP6_0	AP	STXD/ATA_D11/USBH2_D6/TD_11/ARM_CRASID7MCU1_23	I/O	NVCC10	MCIMX31
E9	119	AP6_1	AP	SRXD6/ATA_D12/USBH2_D7/TD_12/M3IF_CHSN_MSTR_0/MC	I/O	NVCC10	MCIMX31

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
				U1_24			
G9	120	AP6_2	AP	SFS6/USBH1_SUSPEND/TD_14/ M3IFCHSN_MSTR_2/MCU1_26	I/O	NVCC10	MCIMX31
G10	121	AP6_3	AP	SCK6/ATA_D13/TD_13/M3IF_CHSN_MSTR_1/MCU1_25	I/O	NVCC10	MCIMX31
V7	212	ASSPI0	AP	SECCS	I/O	LV	MC13783
V9	213	ASSPI1	AP	SECCLK	I/O	LV	MC13783
W14	214	ASSPI2	AP	SECMOSI	I/O	LV	MC13783
Y16	215	ASSPI3	AP	SECMISO	I/O	LV	MC13783

Table 5-13: Connector Sub-Symbol M

5.1.14 Sub Symbol N – Power Group

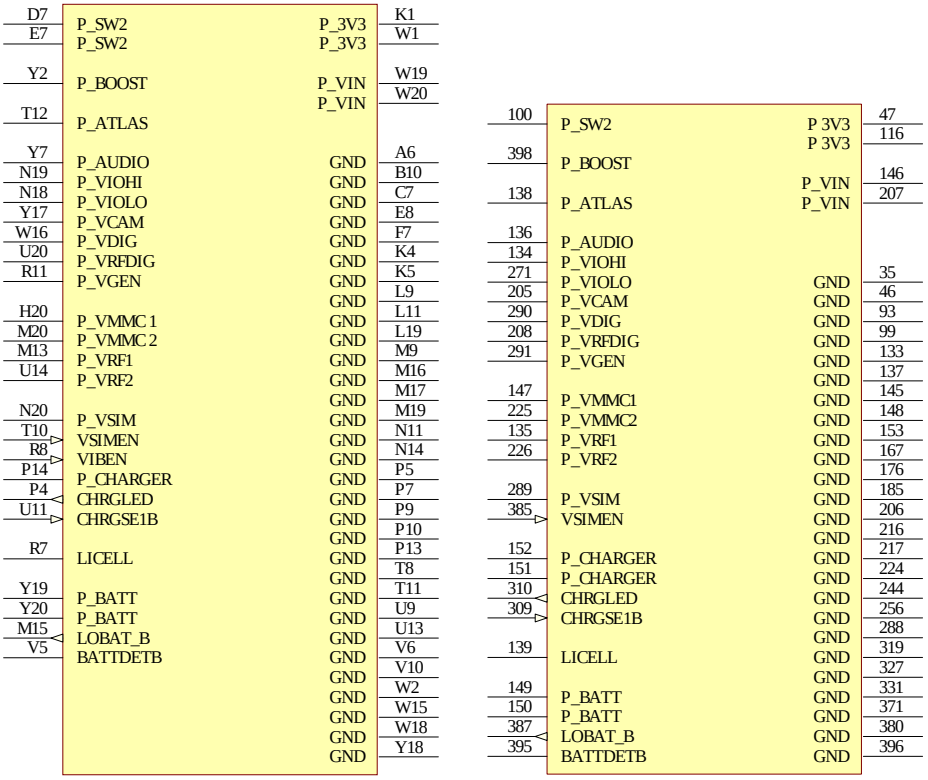

Figure 5-14: Connector Sub-Symbol N

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
V5	395	BATTDETB	Power	BATTDETB	PWR	-	MC13783
P4	310	CHRGLED	Power	CHRGLED	PWR	-	MC13783
U11	309	CHRGSE1B	Power	CHRGSE	PWR	-	MC13783
R7	139	LICELL	Power	LICELL	Passiv	MV	MC13783
M15	387	LOBAT B	Power	LOBATB	O	-	MC13783
K1	116	P_3V3	Power	3.3V +/- 10%	PWR	-	-
W1	47	P_3V3	Power	3.3V +/- 10%	PWR	-	-
T12	138	P_ATLAS	Power	2.775V	PWR	-	-

Y7	136	P_AUDIO	Power	2.775V	PWR	-	-
Y19	150	P_BATT	Power	Battery supply	PWR	-	-
Y20	149	P_BATT	Power	- “ -	PWR	-	-
Y2	398	P_BOOST	Power	5.0V to 5.5V	PWR	-	-
P14	151	P_CHARGER	Power	Input supply max. 20V!	PWR	-	-
-	152	P_CHARGER	Power	- “ -	PWR	-	-
D7	-	P_SW2	Power	0.9V to 2.2V	PWR	-	-
E7	100	P_SW2	Power	0.9V to 2.2V	PWR	-	-
Y17	205	P_VCAM	Power	1.5V to 3.0V	PWR	-	-
W16	290	P_VDIG	Power	1.2V to 1.8V	PWR	-	-
R11	291	P_VGEN	Power	1.2V to 2.4V	PWR	-	-
W19	207	P_VIN	Power	Output from Atals Control 2.8 to 4.65V	PWR	-	-
W20	146	P_VIN	Power	- “ -	PWR	-	-
N19	134	P_VIOHI	Power	2.775V	PWR	-	-
N18	271	P_VIOLO	Power	1.2V to 1.8V	PWR	-	-
H20	147	P_VMMC 1	Power	1.6V to 3.0V	PWR	-	-
M20	225	P_VMMC2	Power	1.6V to 3.0V	PWR	-	-
M13	135	P_VRF1	Power	1.5V to 2.775V	PWR	-	-
U14	226	P_VRF2	Power	1.5V to 2.775V	PWR	-	-
U20	208	P_VRFDIG	Power	1.2V to 1.875V	PWR	-	-
N20	289	P_VSIM	Power	1.8V or 2.9V	PWR	-	-
R8	-	VIBEN	Power		I		
T10	385	VSIMEN	Power	-	I	-	-
A6, B10, C7, E8, F7, K4, K5, L9, L11, L19, M9, M16, M17, M19, N11, N14, P5, P7, P9, P10, P13, T8, T11, U9, U13, V6, V10, W2, W15, W18, Y2, Y18,	35, 46, 93, 99, 133, 137, 145, 148, 153, 167, 176, 185, 206, 216, 217, 224, 244, 256, 288, 319, 327, 331, 371, 380, 396	GND	Power	-	PWR	-	-

Table 5-14: Connector Sub-Symbol N

5.1.15 Sub Symbol O – Miscellaneous Control Group

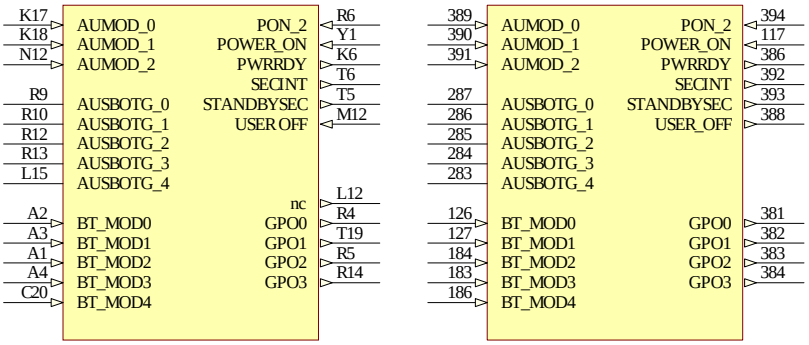

Figure 5-15: Connector Sub-Symbol O

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
K17	389	AUMOD_0	Control	UMOD1	I	LV	MC13783
K18	390	AUMOD_1	Control	UMOD0	I	LV	MC13783
N12	391	AUMOD_2	Control	USBEN	I	LV	MC13783
R9	287	AUSBOTG_0	Control	UID	Passive	EMV	MC13783
R10	286	AUSBOTG_1	Control	UDP	Passive	EMV	MC13783
R12	285	AUSBOTG_2	Control	UDM	Passive	EMV	MC13783
R13	284	AUSBOTG_3	Control	VUSB/VBUS	Passive	-	MC13783
L15	283	AUSBOTG_4	Control	VINBUS	Passive	-	MC13783
A2	126	BT_MOD0	Control	BT_MD0	I	NVCC1	MCIMX31
A3	127	BT_MOD1	Control	BT_MD1	I	NVCC1	MCIMX31
A1	184	BT_MOD2	Control	BT_MD2	I	NVCC1	MCIMX31
A4	183	BT_MOD3	Control	BT_MD3	I	NVCC1	MCIMX31
C20	186	BT_MOD4	Control	BT_MD4	I	NVCC1	MCIMX31
L12	-	nc					
R4	381	GPO0	Control	GPO0	O	LV	MC13783
T19	382	GPO1	Control	GPO1	O	LV	MC13783
R5	383	GPO2	Control	GPO2	O	LV	MC13783
R14	384	GPO3	Control	GPO3	O	LV	MC13783
R6	394	PON_2	Control	ON2_B	I	LV	MC13783
Y1	117	Power_ON	Control	ON1_B	I	LV	MC13783
K6	386	PWRRDY	Control	PWRDY	O	LV	MC13783
T6	392	SECINT	Control	SECINT	O	LV	MC13783
T5	393	STANDBYSEC	Control	STANDBYSEC	O	LV	MC13783
M12	388	USER_OFF	Control	USER_OFF	O	LV	MC13783

Table 5-15: Connector Sub-Symbol O

5.1.16 Sub Symbol P – CSPI Group

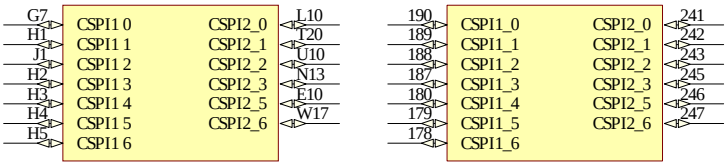

Figure 5-16: Connector Sub-Symbol P

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
G7	190	CSPI1_0	CSPI	CSPI1_MOSI/ATA_D0/ATA_INTRQ/USBH1_RXDM/UART_RXD/TD_15	I/O	NVCC10	MCIMX31
H1	189	CSPI1_1	CSPI	CSPI1_MISO/ATA_D1/ATA_BUFFER_EN/USBH1_RXDP/UART_TXD/TD_16	I/O	NVCC10	MCIMX31
J1	188	CSPI1_2	CSPI	CSPI1_SS2/ATA_D4/ATA_DA1/USBH1_RCV/CSPI3_SS3/TD_19	I/O	NVCC10	MCIMX31
H2	187	CSPI1_3	CSPI	CSPI1_SS1/ATA_D3/ATA_DA0/USBH1_TXDP/CSPI2_SS3/TD_18	I/O	NVCC10	MCIMX31
H3	180	CSPI1_4	CSPI	CSPI1_SS0/ATA_D2/ATA_DMARQ/USBH1_TXDM/CSPI13_SS2/TD_17	I/O	NVCC10	MCIMX31
H4	179	CSPI1_5	CSPI	CSPI1_SCLK/ATA_D5/ATA_DA2/USBH1_OEB/UART3_RTS	I/O	NVCC10	MCIMX31
H5	178	CSPI1_6	CSPI	CSPI1_SPI_RDY/ATA_D6/USBH1_FS/UART3_CTS	I/O	NVCC10	MCIMX31
L10	241	CSPI2_0	CSPI	CSPI2_MOSI/I2C2_SCL	I/O	NVCC10	MCIMX31
T20	242	CSPI2_1	CSPI	CSPI2_MISO/I2C2_SDA	I/O	NVCC10	MCIMX31
U10	243	CSPI2_2	CSPI	CSPI2_SS2/I2C3_SDA/IPU_FLS_STRB	I/O	NVCC10	MCIMX31
N13	245	CSPI2_3	CSPI	CSPI2_SS1/CSPI3_SS1/CSPI1_SS3	I/O	NVCC10	MCIMX31
E10	246	CSPI2_5	CSPI	CSPI2_SCLK/I2C3_SCL	I/O	NVCC10	MCIMX31
W17	247	CSPI2_6	CSPI	CSPI2_SPI_RDY	I/O	NVCC10	MCIMX31

Table 5-16 5-17: Connector Sub-Symbol P

5.1.17 Sub Symbol Q - Audio Group

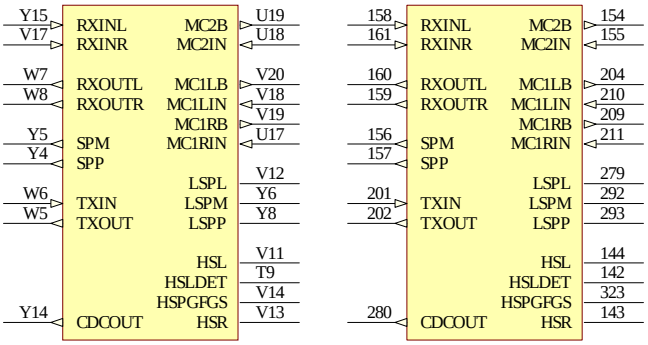

Figure 5-17: Connector Sub-Symbol Q

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
Y14	280	CDCOUT	audio	CDCOUT	O	LV	MC13783
V11	144	HSL	audio	HSL	Passive	-	MC13783
T9	142	HSLDET	audio	HSLDET	Passive	-	MC13783
V14	323	HSPGFGS	audio	HSPGFGS	Passive	-	MC13783
V13	143	HSR	audio	HSR	Passive	-	MC13783
V12	279	LSPL	audio	LSPL	Passive	-	MC13783
Y6	292	LSPM	audio	LSPM	Passive	-	MC13783
Y8	293	LSPP	audio	LSPP	Passive	-	MC13783
V20	204	MC1LB	audio	MC1LB	O	-	MC13783
V18	210	MC1LIN	audio	MC1LIN	I	-	MC13783
V19	209	MC1RB	audio	MC1RB	O	-	MC13783
U17	211	MC1RIN	audio	MC1RIN	I	-	MC13783
U19	154	MC2B	audio	MC2B	O	-	MC13783
U18	155	MC2IN	audio	MC2IN	I	-	MC13783
Y15	158	RXINL	audio	RXINL	I	-	MC13783
V17	161	RXINR	audio	RXINR	I	-	MC13783
W7	160	RXOUTL	audio	RXOUTL	O	-	MC13783
W8	159	RXOUTR	audio	RXOUTR	O	-	MC13783
Y5	156	SPM	audio	SPM	O	-	MC13783
Y4	157	SPP	audio	SPP	O	-	MC13783
W6	201	TXIN	audio	TXIN	I	-	MC13783
W5	202	TXOUT	audio	TXOUT	O	-	MC13783

Table 5-18: Connector Sub-Symbol Q

5.1.18 Sub Symbol R – Ethernet Group

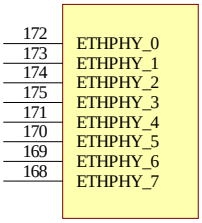

Figure 5-18: Connector Sub-Symbol R

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
-	172	ETHPHY_0	Ethernet	RX_P	Passive		LAN9210/11
-	173	ETHPHY_1	Ethernet	RX_N	Passive		LAN9210/11
-	174	ETHPHY_2	Ethernet	TX_P	Passive		LAN9210/11
-	175	ETHPHY_3	Ethernet	TX_N	Passive		LAN9210/11
-	171	ETHPHY_4	Ethernet	LED1	Passive		LAN9210/11
-	170	ETHPHY_5	Ethernet	LED2	Passive		LAN9210/11
-	169	ETHPHY_6	Ethernet	AGND	Passive		LAN9210/11
-	168	ETHPHY_7	Ethernet	AVDD	Passive		LAN9210/11

Table 5-19: Connector Sub-Symbol R

5.1.19 Sub Symbol S – Shield Group

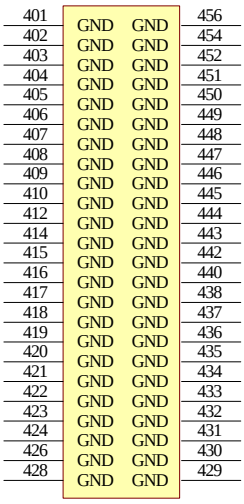

Figure 5-19: Connector Sub-Symbol S

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
-	401-410, 412, 414-424, 426, 428-438, 440, 442-452, 454, 456	GND	Power	Shield	PWR	-	-

Table 5-20: Connector Sub-Symbol S

5.1.20 Sub Symbol (R) T – USB-OTG Group

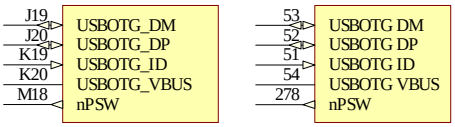

Figure 5-20: Connector Sub-Symbol (R) T

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
J19	53	USBOTG_DM	USB	USBOTG_DM	I/O	-	ISP1504
J20	52	USBOTG_DP	USB	USBOTG_DP	I/O	-	ISP1504
K19	51	USBOTG_ID	USB	USBOTG_ID	I	-	ISP1504
K20	54	USBOTG_VBUS	USB	USBOTG_VBUS	PWR	-	ISP1504
M18	278	nPSW	USB	Pin from ISP1504	O	-	ISP1504

Table 5-21: Connector Sub-Symbol T

5.1.21 Sub Symbol (S) U - FPGA

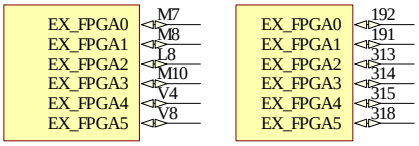

Figure 5-21: Connector Sub-Symbol (S) U

Ball	Pin	Pin Name	Group	Description	Signal type	Power Domain	Chip
M7	192	EX_FPGA0	FPGA	FPGA GPIO 0	I/O	3V3	MACHXO
L8	313	EX_FPGA2	FPGA	FPGA GPIO 1	I/O	3V3	MACHXO
M8	191	EX_FPGA1	FPGA	FPGA GPIO 2	I/O	3V3	MACHXO
M10	314	EX_FPGA3	FPGA	FPGA GPIO 3	I/O	3V3	MACHXO
V4	315	EX_FPGA4	FPGA	FPGA GPIO 4	I/O	3V3	MACHXO
V8	318	EX_FPGA5	FPGA	FPGA GPIO 5	I/O	3V3	MACHXO

Table 5-22: Connector Sub-Symbol (S) U

6 Level Shifting

On the Core Module there are used three types of level shifters:

- Unidirectional level shifters
- Bidirectional level shifters
- Dual powered FPGA

6.1 Dual powered FPGA

The Lattice MachXO LCMXO256 is a FPGA with two IO-banks and a different IO-voltage supply each. Therefore the FPGA is an ideal component for level shifting and allows also a tiny logic circuit implementation.

The following section describes the default FPGA configuration. Upon request, customized FPGA configuration with IP cores (UART 16550), can be designed.

6.1.1 Overview

Figure 6-1: FPGA Overview

Error! Reference source not found. shows the FPGA interconnection on the Core Module. The left side represents the low voltage domain where the i.MX31 signals are connected, the right side represents the high voltage signals routed to the connector with 3.3V logic levels.

6.1.2 External Signal Description

6.1.2.1 Processor Side

Name	Function	Reset State	Type
CS_3	DA bus CS_3	-	Input
CS_4	DA bus CS_4	-	Input
OE_B	DA bus OE	-	Input
RW_B	DA bus RW	-	Input

Name	Function	Reset State	Type
LBA_B	DA bus LBA	-	Input
A[21,20,3..0]	DA address lines	-	Input
D[15..0]	DA data bus	Hi-Z	Tri-state IO
IPU_17	IPU_17 is be used for interrupt (default)	1	Output
UART1_2	UART1_2 can be used for interrupt	-	Hi-Z
UART1_3	UART1_3 can be used for interrupt	-	Hi-Z
UART2_0	UART2_0 can be used for interrupt	-	Hi-Z
MCU1_15_SEL	MCU1_15_SEL is the Enabled for the Core Modul NAND Flash if Rxxx (TBD) is not mounted!	1	Output
MCU1_15	MCU1_15 for the NAND Flash control	-	Input
RESET_B	Reset line for FPGA	-	Input

Table 6-1: i.MX signals connected to the FPGA

6.1.2.2 External Device Side

Name	Function	Reset State	Type
LS_INT	Interrupt line for Ethernet (connector)	-	Input
LS_CS_4	CS for Ethernet (connector)	1	Output
LS_OE_B	DA bus OE	1	Output
LS_RW_B	DA bus RW	1	Output
LS_LBA_B	DA bus LBA	1	Output
LS_B_CLK	DA bus B_CLK	1	Ouput
LS_A[21,20,3..0]	DA address lines	0	Output
LS_D[15..0]	DA data bus	Hi-Z	Tri-state IO
EX_FPGA[5..0]	Extended FPGA function pins	Hi-Z	Hi-Z (see function on state controller)

Table 6-2: FPGA signals routed to the connector

6.2 Static Level Shifting

A simple buffer is used for level shifting from 1.8V to 3.3V in only one direction. The static level shifting is used for the following lines: OE_B, RW_B, B_CLK, LBA_B, A[21,20,3..0].

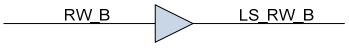

Figure 6-2: Static level shifting example for RW_B

Processor Side	External Device Side
OE_B	LS_OE_B
RW_B	LS_RW_B
B_CLK	B_CLK
LBA_B	LBA_B

Processor Side	External Device Side
A[21,20,3..0]	LS_A[21,20,3..0]

Table 6-3: Static Level Lines

6.3 Dynamic Level Shifting on Data Bus

The level shifting on the data bus is controlled by a direction signal shown in Figure 6-3: Dynamic Level Shifting (DIR – internal in the FPGA)

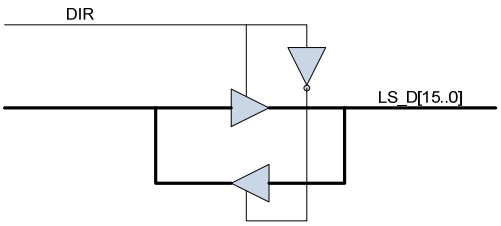

Figure 6-3: Dynamic Level Shifting

6.4 Device Extender

The Device Extender supports two devices on the 3.3V level site, one starting at 0xB400_0000 and the other one starting at 0xB420_000. Each device has its Interrupt line on the 3.3V level side, on the i.MX27 side the Interrupt lines are connected with logical OR (for active low interrupts).

Device	Start Address	Signal Name	External Signal	Processor Signal
A	0xB400'0000	CS	EX_FPGA0	CS3_B
		IRQ	EX_FPGA1	IPU_17
B	0xB420'0000	CS	LS_CS4_B	CS4_B
		IRQ	LS_INT	IPU_17

Table 6-4: Device extension

7 Mount Options

7.1 Component Mount Options

Note: Special mount options are only available for high volume orders. Contact Bluetechnix for Samples or customized Board requests.

For all available Core Module options see the Bluetechnix CM-i.MX31 Selection Guide and the Variants Overview (chapter 14.1).

7.2 0R Mount Options

Different mount option as default upon request.

7.2.1 Special i.MX control signals

Resistor mount options are available for the default voltage level of the SJC_MOD, CLKSS and CE_CONTROL signal.

Table 7-1: i.MX Mount Options

7.2.2 Special MC13783 control signals

The follow table give an overview about the resistor mounting options between the MC13783 and the i.MX3x Processor.

Description	Designator	Default	Function
PWRRDY(MCI3783) to MCU1_1(i.MX)	R32	POP	Short
USEROFF(MCI3783) to MCU1_0(i.MX)	R33	POP	Short
CLKSEL(MCI3783) to P_ATLAS(i.MX)	R34	POP	Short
PRINT(MCI3783) to MCU1_3(i.MX)	R42	POP	Short
LOBAT(MCI3783) to MCU1_4(i.MX)	R43	POP	Short
REGEN(MCI3783) to MCU3_1(i.MX)	R63	POP	Short
SECUCC(MCI3783) to P_SW2(i.MX)	R45	DNP	Short
PUMS3(MCI3783)	R50	DNP	Pull Up
	R49	DNP	Pull Down
PUMS2(MCI3783)	R52	DNP	Pull Down
	R51	POP	Pull Up
PUMS1(MCI3783)	R54	POP	Pull Up
	R53	DNP	Pull Down
P_VIOLO to USBUCC(MCI3783)	R108	DNP	Short
P_VIOHI to USBUCC(MCI3783)	R120	POP	Short
DVFS0(i.MX) to DVS_SW1A(MCI3783)	R79	DNP	Short
DVFS1 to DVS_SW1A	R80	DNP	Short
DVFS0 to DVS_SW1B	R81	DNP	Short
DVFS1 to DVS_SW1B	R82	DNP	Short
DVFS0 to DVS_SW2A	R83	DNP	Short
DVFS1 to DVS_SW2A	R85	POP	Short
DVFS0 to DVS_SW2B	R87	POP	Short
DVFS1 to DVS_SW2B	R88	DNP	Short

Table 7-2: Mount options for MC13783

7.2.3 Misc configuration options

Designator	Default	Description
R127	POP	CKIH to 26MHz
R111	POP	RESET_B(ISP1504) to Reset
R1	POP	26MHz to CLIA
R6	POP	CLIA to CLIB

Table 7-3: special clock and control settings

Designator	Default	Description
R101	POP	P_VBKUP2 to P_GT1 or/and P_SW1
R99	POP	P_GT1 to P_VBKUP2 or/and P_SW1
R98	POP	P_SW1 to P_VBKUP2 or/and P_GT1

Table 7-4: Power Gating

8 Example Schematics

The following schematics are suggestions of how to realise standard applications with the CM-i.MX31 Core Module.

8.1 Minimal System Configuration

The following schematics represent a minimum configuration to get the CM-i.MX31 Core Module running.

8.1.1 Power

Error! Reference source not found. shows the two ways to power the Core Module. The right Picture is the single-supply version; on the left side the charger version is shown.

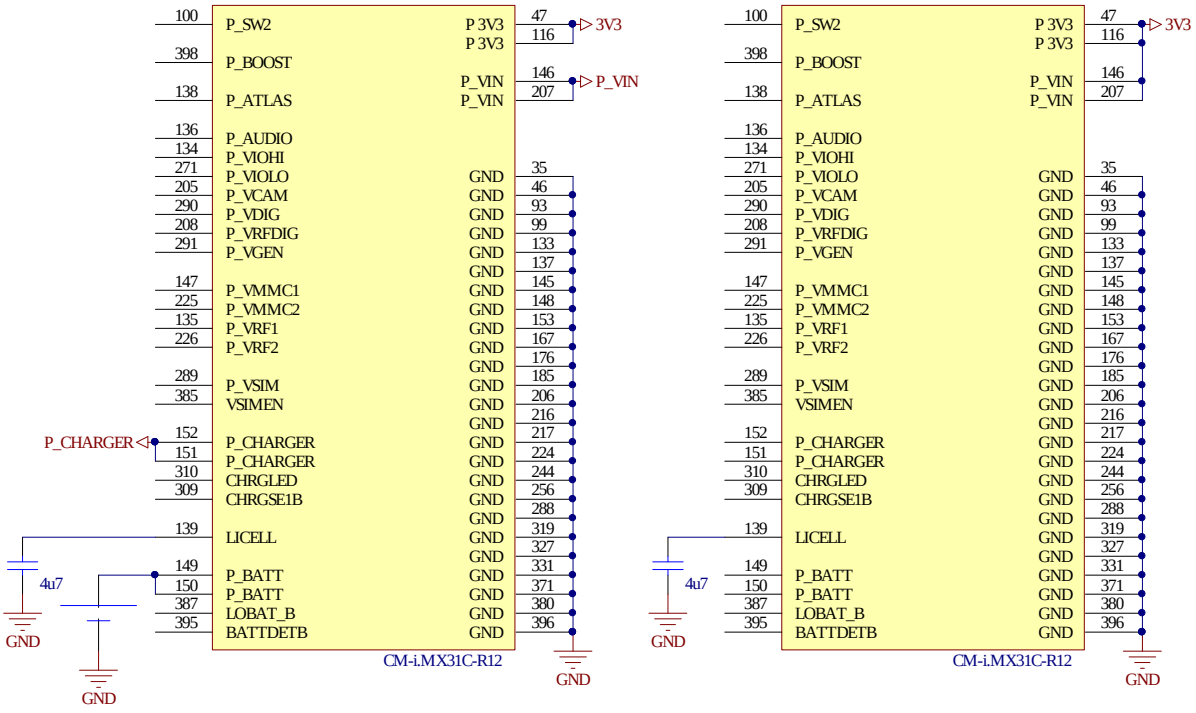

Figure 8-1: Power Schematic

In addition to the 4.7µF capacitor you could connect a lithium based coincell to the LICELL pin. Also a large electrolytic capacitor or a supercap would be a good choice. It is mandatory to connect a minimum capacitor of 4.7µF on LICELL.

More detail information you can find in chapter 2.6 or in the MC13783 user guide.

8.1.2 Charger

A simple schematic for connecting a LiIo battery can be found in the following figure.

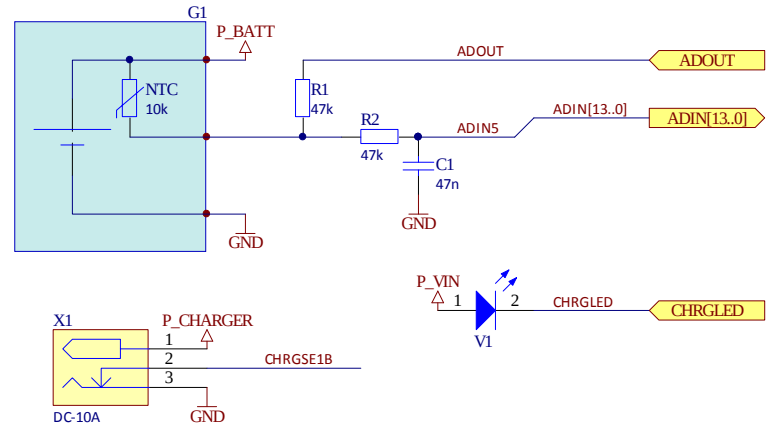

Figure 8-2: Simple charger schematic

If you don't need to observe the temperature of the battery or you don't have a NTC on the battery you can remove R211, R212 and C200. These passive parts are only for measure the temperature for 10k NTC.

8.1.3 Boot Mode

The following picture shows a boot configuration where the CM-i.MX27 is booting from the 16-bit NOR flash. For other boot modes refer to chapter **Error! Reference source not found.**.

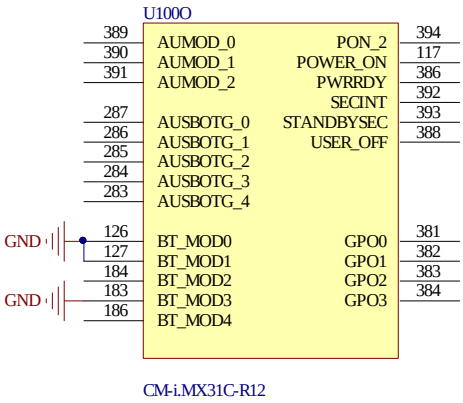

Figure 8-3: Boot Schematic

8.1.4 Reset and JTAG Configuration

This is an example for a simple reset configuration and the wiring information for an ARM JTAG. R311, C302 and U301 are optional and only needed if you connect other devices on RESET_IMX_B.

More information about the clock and reset functionality you can find in chapters **Error! Reference source not found.** and **Error! Reference source not found.**.

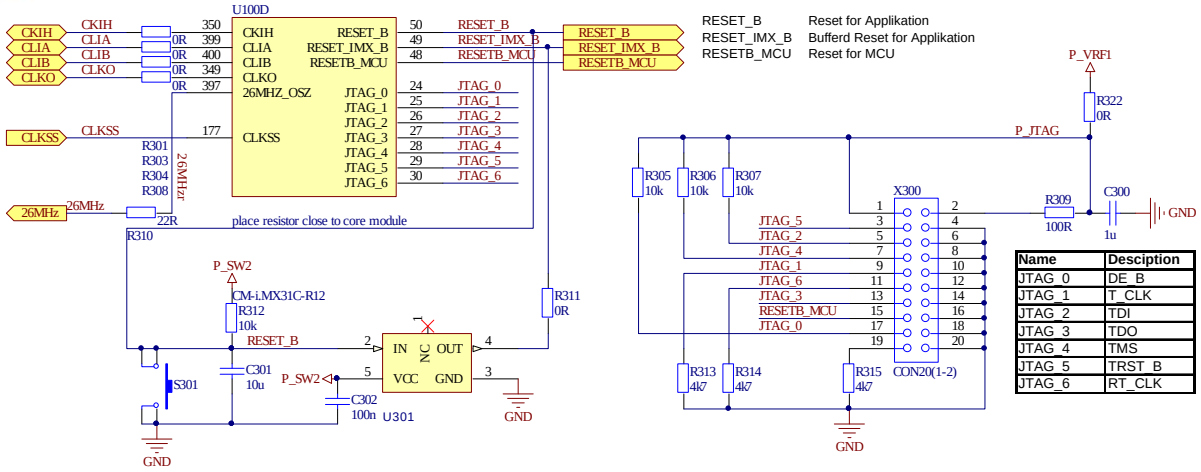

Figure 8-4: Reset configuration with optional JTAG

8.2 Optional Applications

8.2.1 UART Configuration

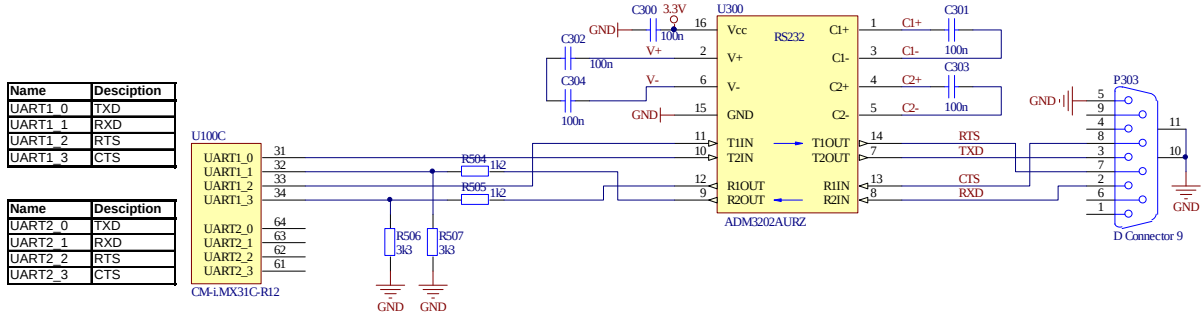

Figure 8-5: Basic UART Schematic

This is a basic UART schematic with an ADM3202 used as a level shifter. This UART can be used as the console UART.

8.2.2 Ethernet Configuration

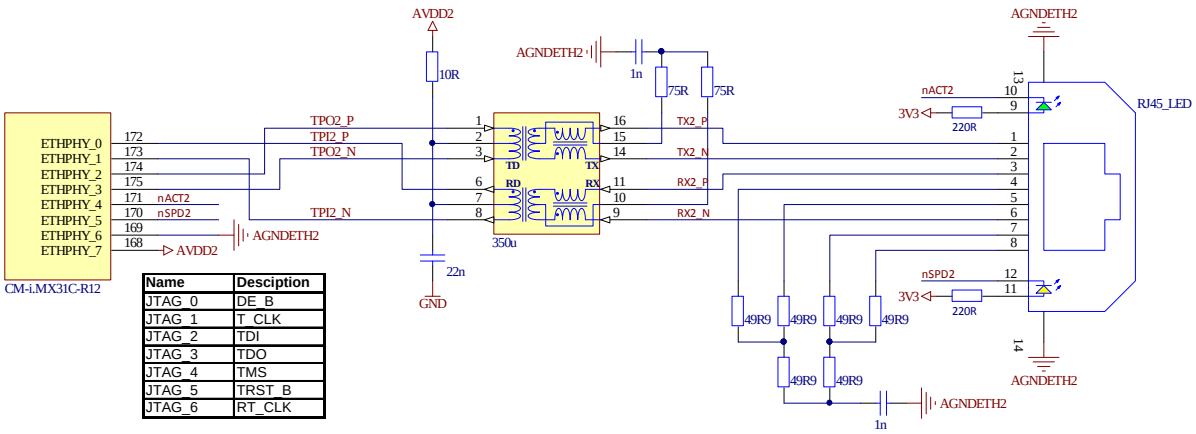

Figure 8-6: Ethernet Schematic

8.2.3 USB OTG Configuration

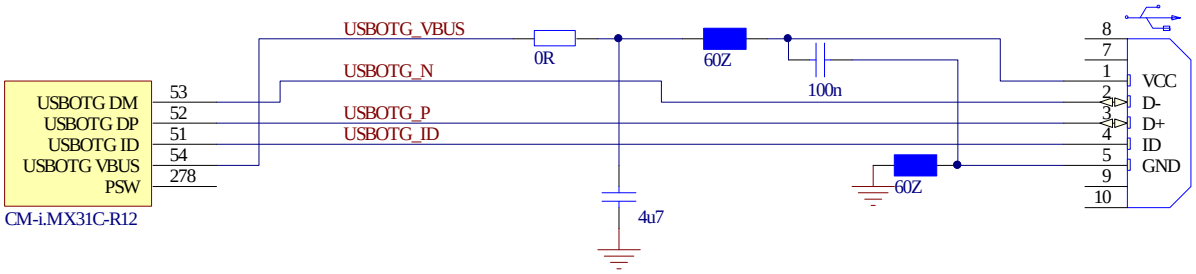

Figure 8-7: Basic USB OTG Schematic

The USB D+ and D- lines are high speed differential signals and should be routed as impedance driven line pairs with a differential impedance of 90Z.

8.2.4 USB OTG as USB Host Configuration

The USB OTG Port can also be used as a USB Host port:

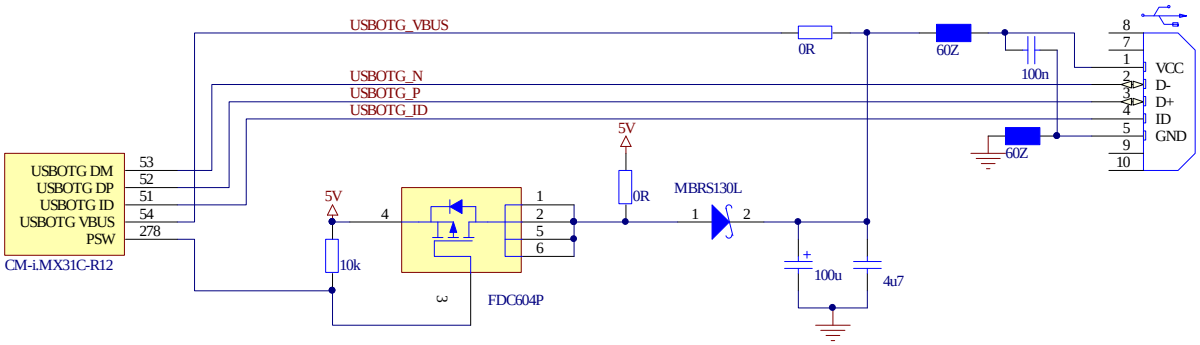

Figure 8-8: USB Host on USB OTG output

It is recommended to use the design rules as described in 8.2.3! Consider that VBUS should be designed for 500mA!

9 Design Verification

9.1 Schematic Design

9.1.1 Check Power Supply Requirements

- Is the power supply within the specified range?
- Is the ripple on P_CHARGER, P_VIN, P_BATT, P_3V3 within the specified range?

9.1.2 Batteries

- Check the Li-Ion Battery voltage (only one cell LiIo Batteries are supported)
- Do you have an LICELL (coincell) in use? If no add a 4u7 capacitor on LICELL pin! Is the voltage range from the coincell within the spec?

9.1.3 Serial Communication

- Check RXD and TXT
- Check CTS and RTS
- Are level shifters needed? (IO voltage level 2.8V!)

9.1.4 USB OTG

- D+ and D- correct?
- ID pin in use?
- External power MOSFET needed?
- ESD protection?

9.1.5 Ethernet

- Termination resistors on RX/TX lines?
- Transformer in specified range?

9.1.6 Boot Modes

- Are the boot mode pins connected for boot up?
- Is it possible to use the Bootstrap boot up mode (e.g. for usage in conjunction with the ATK tool)?

9.2 PCB Layout

- Add a ground plane underneath the Core Module to reduce interference
- Do not place any components underneath the Core Module (Connector Version)
- To reduce interference place ceramic decoupling capacitors on the power supplies near the balls/pins. (100nF)
- Check if the USB lines (D+/D-) have the correct impedance and that they are routed as differential line pairs!
- Check if the Ethernet lines (Rx/Tx) have the correct impedance and that they are routed as differential line pairs!

10 Troubleshooting

10.1 Core Module doesn't start up

Check the following issues:

- boot mode options
- Power supply on P_CHARGER or P_BATT and P_3V3 (see chapter 2.6)

10.2 Battery is not charged

The battery is not charged automatically you have to use the atlas-charger tool. The MA13783 Charger Register has to be set correct. For further details refer the CM-i.MX27 Software Manual.

10.3 Freescale HAB ADS Toolkit doesn't work

Check the following issues:

- Boot Mode Option
- CLKSS state
- UART Communication

11 Soldering (BGA only)

11.1 Soldering Paste

The balls are pumped with 5.1AT Indalloy 244. It is recommended to use solder past which is compatible with Indalloy 244!

11.2 Reflow Soldering

Figure 12-1 shows a proposal for a reflow profile. Please note the profile details (i.e. timing, type of oven) depend upon many parameters, specially the baseboard. They must be tested before on the target reflow oven.

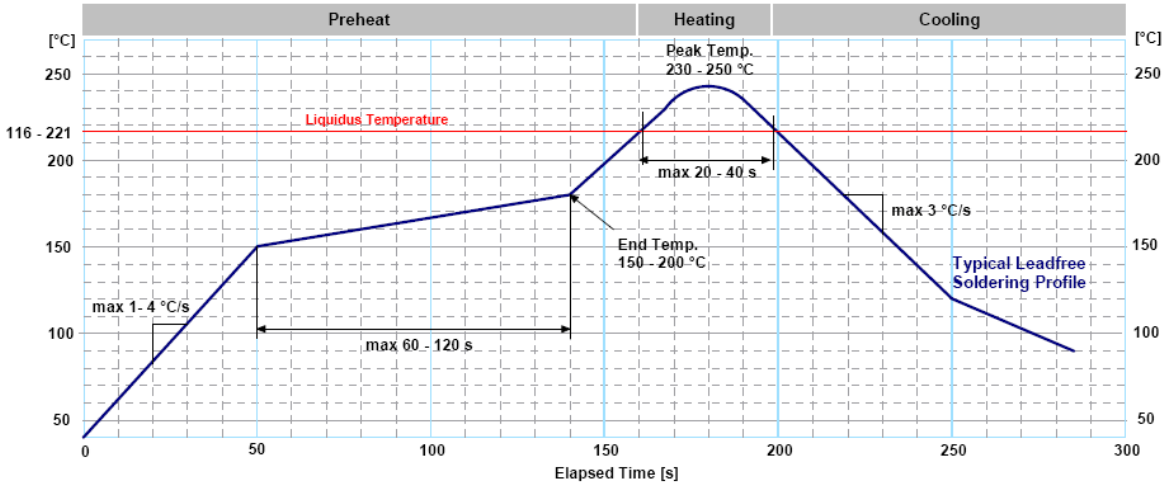

Figure 11-1 Reflow Soldering

11.3 Repeated reflow Soldering

We recommend only a single reflow soldering process with our Core Modules because of the high risk of falling off due to soldering.

11.4 Grounding Metal Covers

The Core Module has a ground ring around the PCB outlines which is connected directly to the GND plane for reducing EMI. Bluetechnix takes no warranty for damages on the Core Module caused by soldering a metal case on our Core Module!

12 Mechanical Stress

Note that excessive twisting while inserting or withdrawing the CM-i.MX31 will damage the connectors.

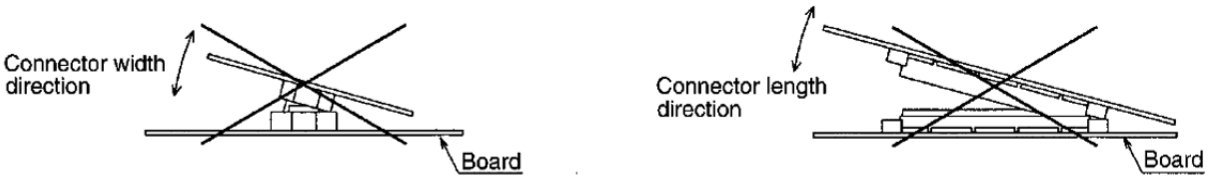

Figure 12-1: Unplugging the Core Module

13 Package Information

13.1 Embossed Carrier Tape Dimensions

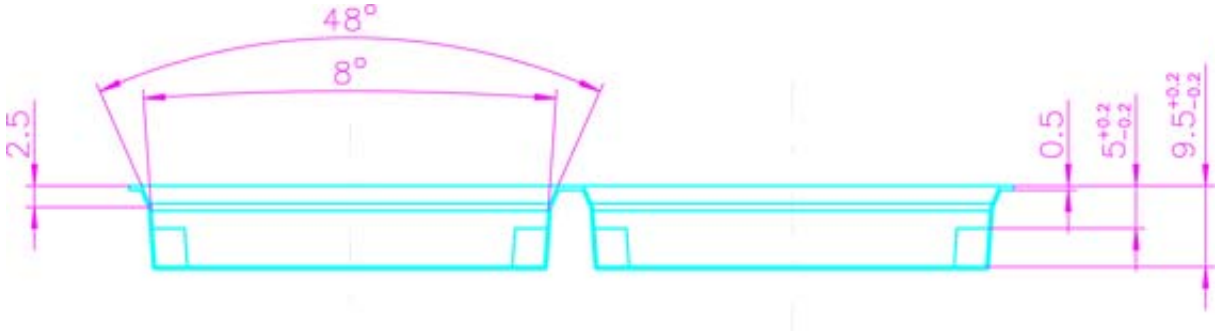

Figure 13-1: Blister side view

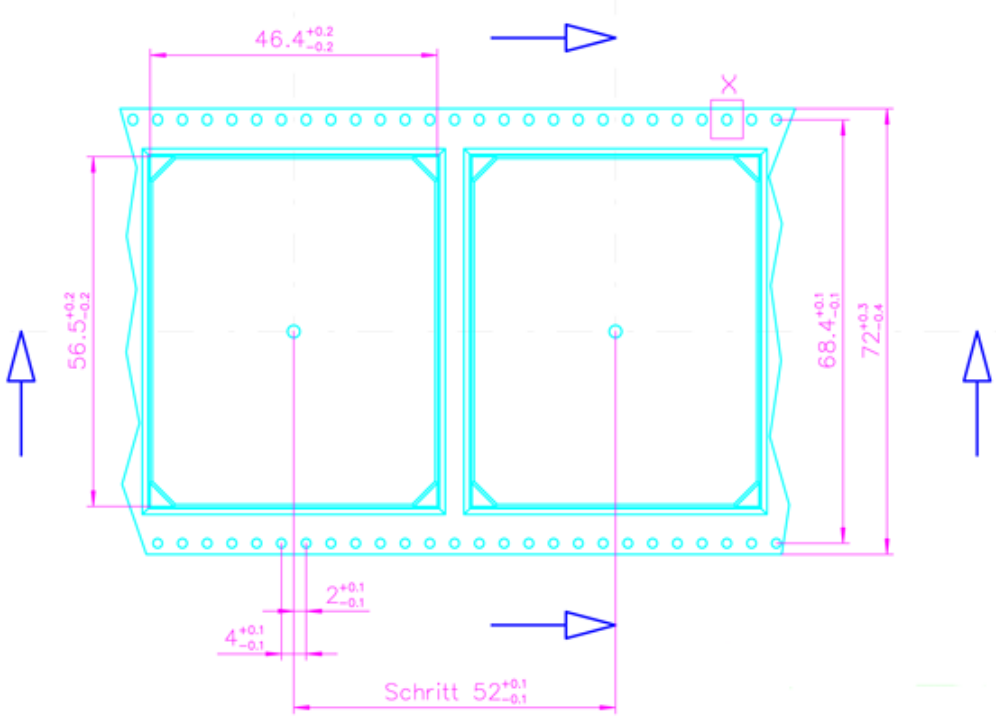

Figure 13-2: Blister top view

13.2 Shipment, Storage and Handling

The CM-i.MX31B Core Module is designed and packaged to be processed in an automatic assembly line. You will get the Core Modules in Tape and Reel packages.

Please take care with the Core Modules, our Core Modules contains highly sensitive electronic circuits. Keep in mind with ESD, JEDEC and ISP. Our Core Modules are according to IPC/JEDEC J-STD-020C and are moisture sensitive devices.

The dry bag provides a JEDEC compliant MSD label (Moisture Sensitive Devices) describing the handling requirements to prevent humidity intake.

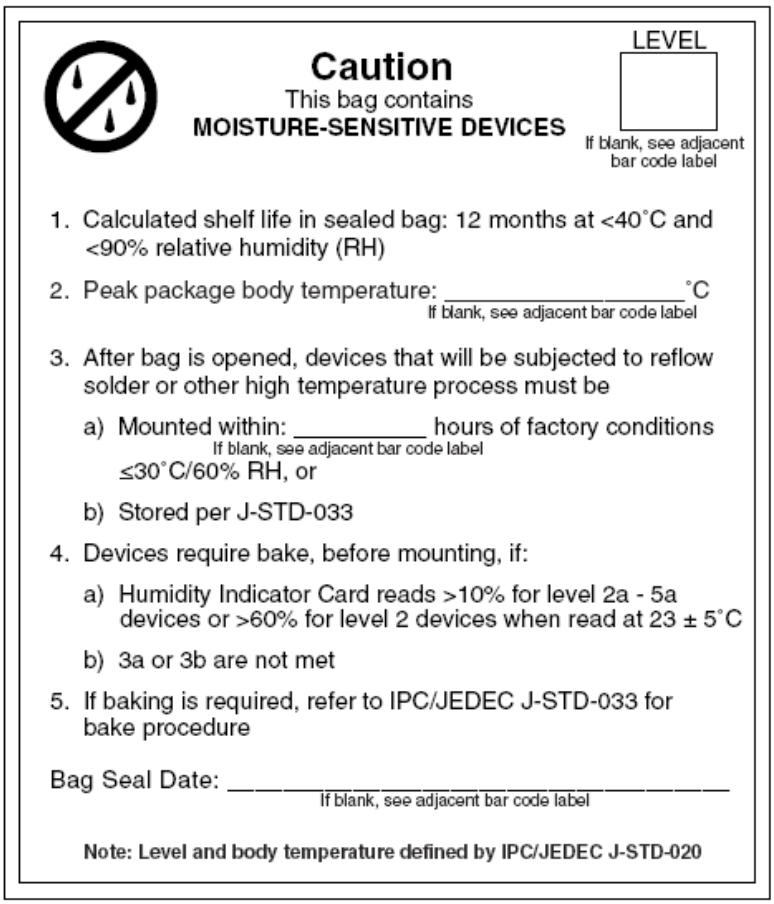

Figure 13-3: Moisture-Sensitive Caution Label

13.3 Storage

Shelf life in a sealed bag is 12 month at <40°C and <90% relative humidity.

13.4 Handling

The Core Modules are shipped on tape-and-reel in a hermetically sealed package which includes a humidity indicator card.

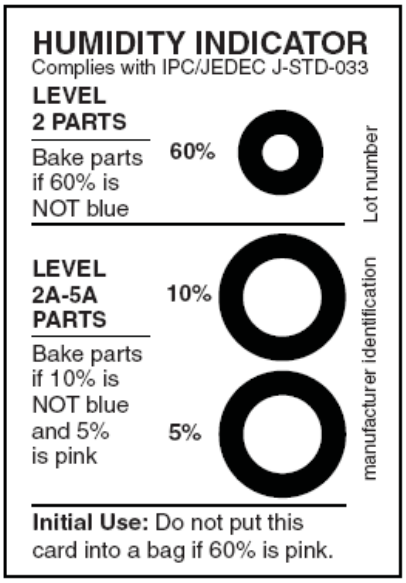

Figure 13-4: Example Humidity Indicator Card

13.5 Floor Life (only BGA)

The Core Module must be processed and soldered within the moisture sensitivity level 4 specifications, where the floor life is given as 72 hours.

Once the sealed package of the reel is opened and the parts exposed to humidity, they need to be processed within 72 hours and a reflow soldering process. If this time is exceeded, the Core Modules have to be pre-baked before used in the flog solder process!

13.6 Recommended baking procedure

Do not attempt to bake the Core Modules contained in tape and rolled up in reels! If you need to bake the Core Modules quickly at 125°C for 48hours, remove them from the belt and place them individually onto the oven tray.

Recommended baking procedure is 48 hours at 125°C below 5% Humidity.

14 Order Information

14.1 Variants Overview

Module	CPU	Mobile DDR-SDRAM	Combo Chip	NOR Flash Intel P30	NAND Flash	Ethernet Controller	FPGA	Level Shifter	USB OTG	Power Supply	Connector
CM-i.MX31B-AA	i.MX31	128MB 32bit	32MB NOR Flash; 16MB PSRAM	not possible	128MB	not possible	yes	yes	yes	MC13783	not possible
CM-i.MX31B-AB	i.MX31L	64MB 32bit	32MB NOR Flash; 16MB PSRAM	not possible	128MB	not possible	yes	yes	yes	MC13783	not possible
CM-i.MX31B-AF	i.MX31L	64MB 32bit	32MB NOR Flash only	not possible	no	not possible	no	no	yes	MC13783	not possible
CM-i.MX31C-AA	i.MX31	128MB 32bit	32MB NOR Flash; 16MB PSRAM	8MB	128MB	LAN9211	yes	yes	yes	MC13783	400 pin
CM-i.MX31C-AC	i.MX31L	64MB 32bit	no	8MB	128MB	LAN9210	yes	yes	yes	MC13783	400 pin
CM-i.MX31C-AE	i.MX31	128MB 32bit	32MB NOR Flash only	8MB	no	LAN9211	yes	yes	yes	MC13783	400 pin

Table 14-1: Most common mounting options

For standard mounting see **Error! Reference source not found.**.

14.2 Order Code

Please contact Bluetechnix for detailed ordering information.

15 Anomalies

For the latest up-to-date information about this product, please consult the product homepage: www.bluetechnix.com/goto/cm-i.mx31c

15.1 Erratum 1: SOM might hang when ehci-hcd driver is loaded

Description	If specific input data is presented to the module and the reset line is currently active, loading the driver fails and the module seems to hang. This issue occurs infrequently (~ 1% of the time) and is not reproducible.
Date	April, 2009
Affects	All i.MX31 Core Modules including (but not limited to) revision 1.2.1.
Status	Issue confirmed and resolved.
Workaround	Hardware workaround is needed. Please contact Bluetechnix.

15.2 Erratum 2: SOM might hang when ehci-hcd driver is loaded and USB Host 2 is used

Description	If specific input data is presented to the module during reset and USB Host 2 was selected in the kernel configuration the module might lock up when loading the ehci-hcd driver. This issue occurs infrequently and is not reproducible.
Date	July, 2009
Affects	All i.MX31 Core Modules including (but not limited to) revision 1.2.1.
Status	Issue confirmed.
Workaround	If your module was exchanged by Bluetechnix due to Erratum 1, deselect USB Host 2 in the Kernel Configuration and only use the USB OTG port.

16 Product Changes

For the latest information regarding product changes, please consult the product homepage: www.bluetechnix.com/goto/cm-i.mx31c.

Version	Changes
V1.3	USBOTG Transceiver Workaround for ISP1507 bug. Onboard clock routing changed for better signal quality.
V1.2	Fixed RTC power consumption, removed some mount options, moved some component for more space between the components. (e.g. NAND flash)
V1.1	Fixed Bugs on Footprint and Level Shifter, new pinout

Table 16-1: Product Changes

17 Production Report

17.1 CM-i.MX31C (100-1203)

Version	Component	Type
V1.1.2-V1.1.3	Processor	Silicon Rev. 1.2
	MC13783	MC13783VK
	NAND Flash	Micron MT29F1G
V1.1.1	Processor	Silicon Rev. 1.1
	MC13783	MC13783VK
	NAND Flash	ST NAND01G-B2B

Table 17-1: Production Report CM-i.MX31

17.2 CM-i.MX31B (100-1203)

Version	Component	Type
V1.1.2-V1.1.3	Processor	Silicon Rev. 1.2
	MC13783	MC13783VK
	NAND Flash	Micron MT29F1G
V1.1.1	Processor	Silicon Rev. 1.1
	MC13783	MC13783VK
	NAND Flash	ST NAND01G-B2B

Table 17-2: Production Report CM-i.MX31

18 Document Revision History

Version	Date	Document Revision
13	2010-07-13	Changed ordering information
12	2008-07-22	Errata added
11	2008-12-05	Mounting options
10	2008-11-05	Fixed some errors in the pin descriptions (USB2, MCU2_0..3, P_CHARGER, P_Sw2, BT_MOD2..3)
9	2008-08-12	Fix up tables
8	2008-08-11	English checked for grammar and spelling, some parts re-phrased for clarity.
7	2008-08-05	Fix up and Cleaning up
6	2008-02-20	Insert Solder and Packaging
5	2008-02-11	Review Martin Hausner
4	2007-10-07	Wording
3	2007-10-02	Bug fixing
2	2007-09-28	Several updates
1	2007-08-16	Initial Version of the Hardware User Manual

Table 18-1: Revision History

19 List of abbreviations

BGA	Ball Grid Array
USB	Universal Serial Bus
EMI	External Memory Interface
CSPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
I2C	A Multi-master Serial Computer Bus
UART	Universal Asynchronous Receiver/Transmitter
USB OTG	USB On-The-Go
USB LS/FS	USB Low Speed / USB Full Speed
IrDA	Infrared Data Association
MMC/SD	Multi Media Card/Secure Digital Card
PCMCIA/CF	Personal Computer Memory Card Internacional Association/ Compact Flash
SIM	Subscriber Identification Module
ATA	Advanced Technology Attachment
SDRAM/DDR	Synchronous Dynamic Random Access Memory/Double Data Rate SDRAM
NANDF	NAND Flash
PSRAM	Pseudostatic RAM
SDMA	Smart Direct Memory Access
PWM	Pulse-Width Modulation
WD	Watchdog
RTC	Real-Time Clock
GPIO	General Purpose Input/Output
RAM	Random Access Memory
ROM	Read-Only Memory
MPEG	Moving Picture Experts Group
JTAG	Joint Test Action Group (IEEE 1149.1 Standard)
ETM	Embedded Trace Macrocell (ARMs JTAG Extension)

DVS	Dynamic Voltage Scaling
RF	Radio Frequency
ADC	Analog-Digital Converter or Asynchronous Display Controller
PLL	Phase-Locked Loop
OV	Over-Voltage
UV	Under-Voltage
RST	Reset
LCD	Liquid Crystal Display
LED	Light-Emitting Diode
MCP	Multi-Chip Product
FPGA	Field-Programmable Gate Array
PDA	Personal Digital Assistant
POP	Populate
DNP	Do Not Populate
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