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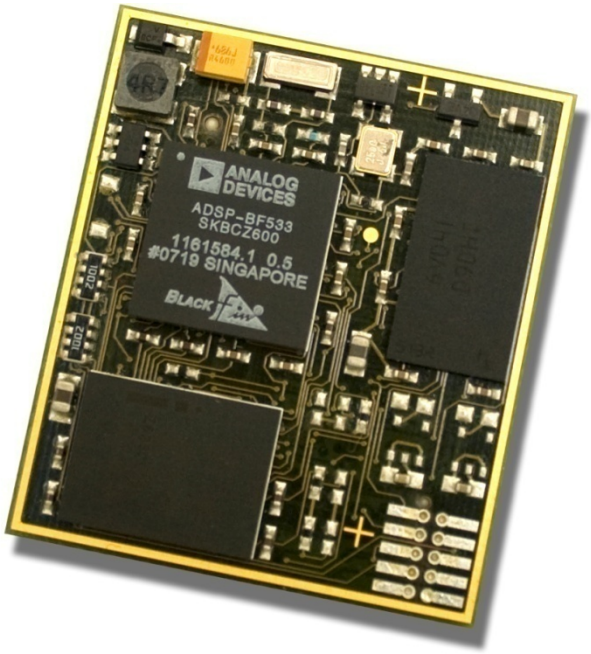

Hardware User Manual

CM-BF533 V2.x

...maximum performance at minimum space

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Table of Contents

1 Introduction 8
1.1 Overview 8
1.2 Key Features 9
1.3 Target Applications 9
1.4 Further Information 9
2 Specification 10
2.1 Functional Specification 10
2.2 Boot Mode 10
2.3 Memory Map 11
2.4 Electrical Specification 11
2.4.1 Supply Voltage 11
2.4.2 Supply Voltage Ripple 11
2.4.3 Input Clock Frequency 11
2.4.4 Real Time Clock Crystal 11
2.4.5 Supply Current 11
2.5 Environmental Specification 11
2.5.1 Temperature 11
2.5.2 Humidity 11
3 CM-BF533 (Connector Version) 12
3.1 Mechanical Outline 12
3.2 Footprint 13
3.3 Top Mounted Connector 14
3.4 Schematic Symbol (Signals of P1 and P2) 15
3.5 Connectors Pin Assignment P1 – (1-60) 16
3.6 Connector Pin Assignment P2 – (61-120) 18
3.7 ITU656 Camera Connector P3 (1-22) 19
3.8 Connector P4 (1-10) 20
3.9 Reset circuit 20
4 Test Points 21
4.1 Footprint – Test Points 21
5 Application Examples 22
5.1 Sample Application 22
5.2 Mini Camera System 23
5.3 Generic Signal Processing System 23

5.4 Coprocessor Application 23
5.5 Digital Video System 23
5.6 Design Services 24
6 Software Support 24
6.1 BLACKSheep 24
6.2 uClinux 24
7 Anomalies 24
8 Production Report for CM-BF533 (100-1203) 24
9 Product Changes 25
10 Document Revision History 25
11 A List of Figures and Tables 26

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Warning

Due to technical requirements components may contain dangerous substances.

The Core Modules and development systems contain ESD (electrostatic discharge) sensitive devices. Electro-static charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused Core Modules and Development Boards should be stored in the protective shipping

BLACKFIN Products

Core Modules:

CM-BF533:	Blackfin Processor Module powered by Analog Devices' single core ADSP-BF533 processor; up to 600MHz, 32MB SDRAM, 2MB flash, 2x60 pin expansion connectors and a size of 36.5x31.5mm.
CM-BF537E:	Blackfin Processor Module powered by Analog Devices' single core ADSP-BF537 processor; up to 600MHz, 32MB SDRAM, 4MB flash, integrated TP10/100 Ethernet physical transceiver, 2x60 pin expansion connectors and a size of 36.5x31.5mm.
CM-BF537U:	Blackfin Processor Module powered by Analog Devices' single core ADSP-BF537 processor; up to 600MHz, 32MB SDRAM, 4MB flash, integrated USB 2.0 Device, 2x60 pin expansion connectors and a size of 36.5x31.5mm.
TCM-BF537:	Blackfin Processor Module powered by Analog Devices' single core ADSP-BF537 processor; up to 500MHz, 32MB SDRAM, 8MB flash, a size of 28x28mm, 2x60 pin expansion connectors, Ball Grid Array or Border Pads for reflow soldering, industrial temperature range -40°C to +85°C.
CM-BF561:	Blackfin Processor Module powered by Analog Devices' dual core ADSP-BF561 processor; up to 2x 600MHz, 64MB SDRAM, 8MB flash, 2x60 pin expansion connectors and a size of 36.5x31.5mm.
CM-BF527:	The new Blackfin Processor Module is powered by Analog Devices' single core ADSP-BF527 processor; key features are USB OTG 2.0 and Ethernet. The 2x60 pin expansion connectors are backwards compatible with other Core Modules.
CM-BF548:	The new Blackfin Processor Module is powered by Analog Devices' single core ADSP-BF548 processor; key features are 64MB DDR SD-RAM 2x100 pin expansion connectors.
TCM-BF518:	The new Core Module CM-BF518 is powered by Analog Devices' single core ADSP-BF518 processor; up to 400MHz, 32MB SDRAM, up to 8MB flash. The 2x60 pin expansion connectors are backwards compatible with other Core Modules.

Development Boards:

EVAL-BF5xx:	Low cost Blackfin processor Evaluation Board with one socket for any Bluetechnix Blackfin Core Module. Additional interfaces are available, e.g. an SD-Card.
DEV-BF5xxDA-Lite:	Get ready to program and debug Bluetechnix Core Modules with this tiny development platform including an USB-Based Debug Agent. The DEV-BF5xxDA-Lite is a low cost starter development system including a VDSP++ Evaluation Software License.
DEV-BF548-Lite:	Low-cost development board with one socket for Bluetechnix CM-BF548 Core Module. Additional interfaces are available, e.g. an SD-Card, USB and Ethernet.

DEV-BF548DA-Lite: Get ready to program and debug Bluetechnix CM-BF548 Core Module with this tiny development platform including an USB-Based Debug Agent. The DEV-BF548DA-Lite is a low-cost starter development system including a VDSP++ Evaluation Software License.

EXT-Boards: The following Extender Boards are available: EXT-BF5xx-AUDIO, EXT-BF5xx-VIDEO, EXT-BF5xx-CAM, EXT-BF5xx-EXP-TR, EXT-BF5xx-USB-ETH2, EXT-BF5xx-AD/DA, EXT-BF548-EXP and EXT-BF518-ETH. Furthermore, we offer the development of customized extender boards for our customers.

Software Support:

BLACKSheep: The BLACKSheep VDK is a multithreaded framework for the Blackfin processor family from Analog Devices that includes driver support for a variety of hardware extensions. It is based on the real-time VDK kernel included within the VDSP++ development environment.

LabVIEW: LabVIEW embedded support for Bluetechnix Core Modules is done by Schmid-Engineering AG: http://www.schmid-engineering.ch

uClinux: All the Core Modules are fully supported by uClinux. The required boot loader and uClinux can be downloaded from: http://blackfin.uClinux.org.

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BLACKFIN Design Service

Based on more than five years of experience with Blackfin, Bluetechnix offers development assistance as well as custom design services and software development.

1 Introduction

The CM-BF533 is a tiny, high performance and low power DSP/RISC core module incorporating Analog Devices Blackfin family of processors. The module allows easy integration into high demanding very space and power limited applications.

1.1 Overview

The Core Module CM-BF533 consists of the following components:

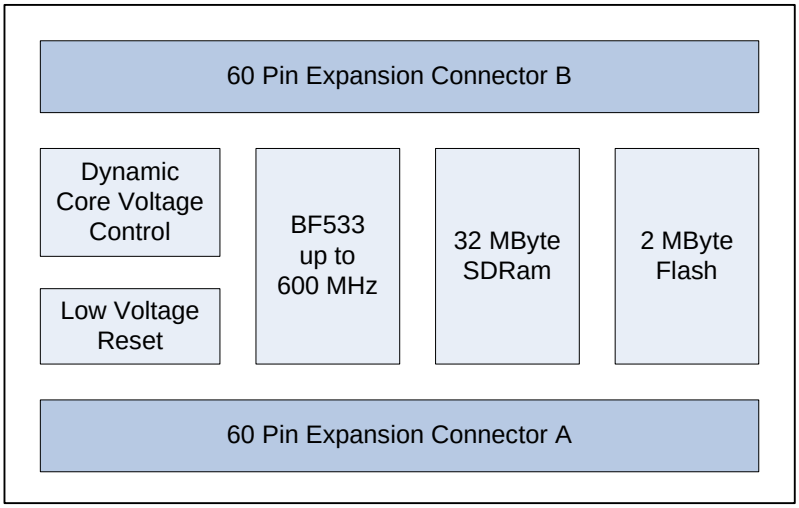

Figure 1-1: Main Components of the CM-BF533 module

- **Analog Devices Blackfin Processor BF533**
  - ADSP-BF533SKBCZ600 (0°-70°C) Standard mount
  - ADSP-BF533SBBCZ500 (-40°-85°C) Option upon request
- **32 MB SDRAM**
  - SDRAM clock up to 133 MHz
  - MT48LC16M16A2BG-7 (16Mx16 at 3.3 V)
- **2MB of Byte Addressable Flash**
  - ITLRC28F320J3C110 (2Mx16 at 3.3 V; 2MByte addressable only)
  - Additionally flash memory can be connected through the expansion board as parallel flash using asynchronous chip select lines or as SPI flash.

- **Low Voltage Reset Circuit**
  - Resets module if power supply goes below 2.93 V for at least 140 ms

- **Dynamic Core Voltage Control**
  - Core voltage adjustable by setting software registers on the Blackfin Processor
  - Core voltage range: 0.8 – 1.32V

- **Expansion Connector A**
  - Data Bus
  - Address Bus
  - Control Signals
  - Power Supply

- **Expansion Connector B**
  - SPORT 0 and SPORT 1
  - JTAG
  - UART
  - SPI
  - PPI (Parallel Port Interface)
  - GPIO's

1.2 Key Features

- The CM-BF533 is very compact and measures only 36.5x31.5mm
- Allows quick prototyping of product that comes very close to the final design
- Reduces development costs, faster time to market
- Very cost effective for small and medium volumes

1.3 Target Applications

- Generic high performance signal processor module
- Internet Connected Embedded System
- High performance web camera
- Robotics: Tiny processor module for mobile robots

1.4 Further Information

Further information, and document updates are available on the product homepage: http://www.bluetechnix.com/goto/cm-bf533

2 Specification

2.1 Functional Specification

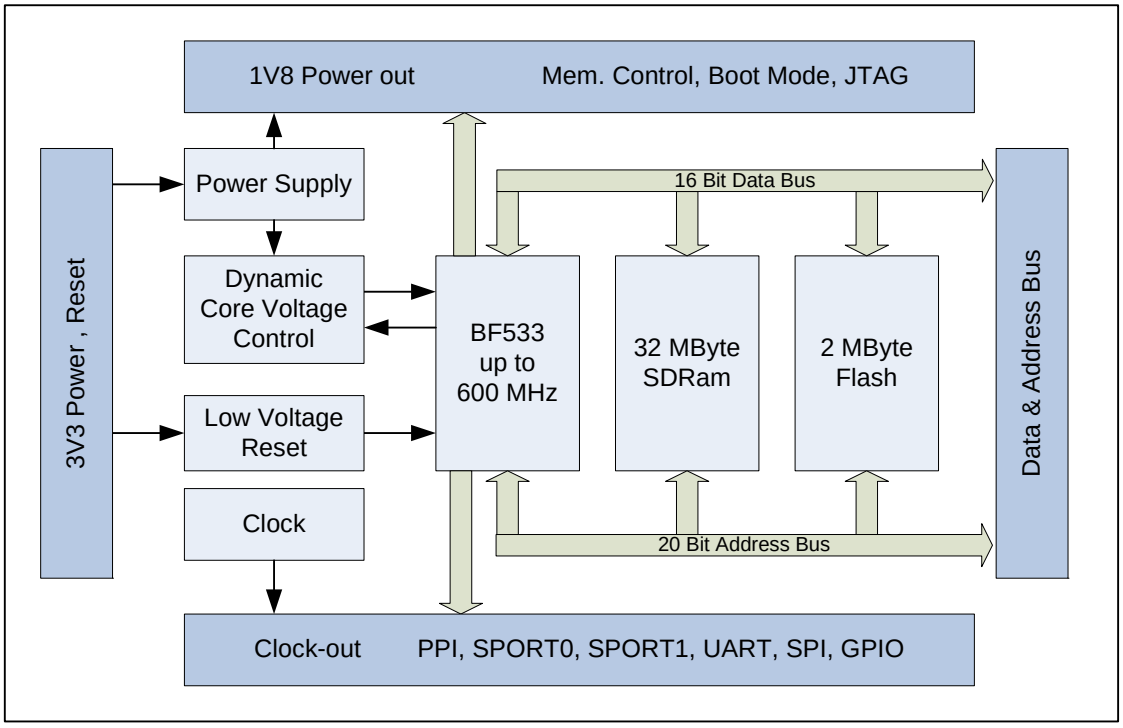

Figure 2-1: Detailed Block Diagram

Figure 2-1 shows a detailed block diagram of the CM-BF533 module. Beside the SDRAM control pins the CM-BF533 has all other pins of the Blackfin processor at its two main 60 pin connectors.

Dynamic voltage control allows reducing power consumption to a minimum adjusting the core-voltage and the clock frequency dynamically in accordance to the required processing power.

A low voltage reset circuit guarantees a power on reset and resets the system when the input voltage drops below 2.93V.

2.2 Boot Mode

Default Boot Mode = 00 (BMODE1 = LOW, BMODE0 = LOW)

BMODE0, BMODE1 has internal pull-down resistor

Connect BMODE0 to Vcc and leave BMODE1 pin open for Boot Mode 01 (equals to 8 or 16 bit PROM/FLASH boot mode), this is the default boot mode of the BLACKSheep software.

See Blackfin ADSP-BF533 Datasheets or Eval/DevBoard manuals for more details.

2.3 Memory Map

Memory Type	Start Address	End Address	Size	Comment
FLASH	0x20000000	0x201FFFFF	2MB	RC28F320J3C110
SDRAM	0x00000000	0x01FFFFFF	32MB	16Bit Bus, Micron MT48LC16M16A2BG-7

Table 2-1: Memory Map

2.4 Electrical Specification

2.4.1 Supply Voltage

- 3.3 V DC +/-10%

2.4.2 Supply Voltage Ripple

- 100 mV peak to peak 0-20MHz

2.4.3 Input Clock Frequency

- 25MHz

The Blackfin Processor Input Clock frequency is 25MHz, this frequency is derived from the on-board crystal/oscillator and drives the Blackfin Processors's Clock generator. This frequency is also provided on the connector as pin 78 (CLK_out).

2.4.4 Real Time Clock Crystal

- 32.768kHz

2.4.5 Supply Current

- Maximum supply current: 250mA @ 3.3V
- Operating conditions:
    - Processor running at 600MHz, Core Voltage 1.2V, SDRAM 20% bandwidth utilization at 130MHz: 150mA
    - Processor running at 300MHz, Core Voltage 0.8V SDRAM 20% bandwidth utilization at 130MHz: 90mA

2.5 Environmental Specification

2.5.1 Temperature

Development Version:

- Operating at full 600MHz: 0 to + 70° C

Industrial Version: (Only available upon request at an MOQ)

2.5.2 Humidity

- Operating: 10% to 90% (non condensing)

3 CM-BF533 (Connector Version)

3.1 Mechanical Outline

TOP VIEW

All dimensions are given in millimeters!

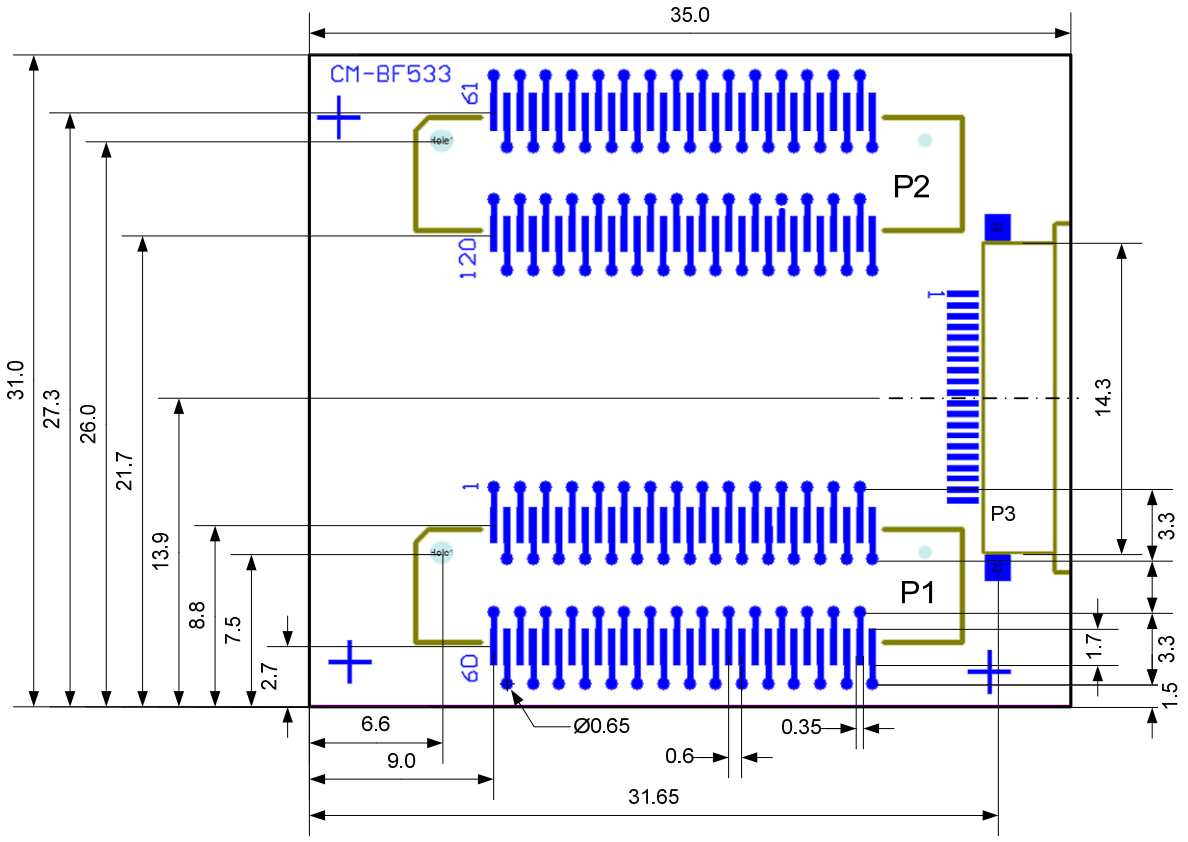

Figure 3-1: Mechanical outline and Bottom Connectors (Top-View)

The mechanical outline represents a top view of the connectors placed at the bottom of the core board.

The module is shipped with two 60pin connectors.

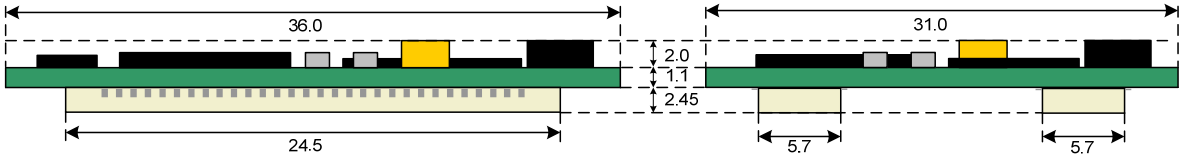

Figure 3-2: Side View with connectors mounted

The total minimum mounting height including receptacle at the motherboard is 6.1 mm.

The connectors on the CM-BF533 are of the following type:

Part	Manufacturer	Manufacturer Part No.
P1,P2	Hirose 3mm height	FX8-60P-SV
P3	Molex (not mounted)	52435-2491
P4 (top)	Harwin (not mounted)	M50-3150522

Table 3-1: Module connector types

3.2 Footprint

If the connector version (2x Hirose 0.6mm pitch) is used, the footprint for the baseboard may look as shown in Figure 3-3.

For the baseboard the following connectors have to be used:

Part Baseboard	Manufacturer	Manufacturer Part No.
P1,P2	Hirose	FX8-60S-SV
P4 (top)	Harwin	M50-3600522

Table 3-2: Baseboard connector types

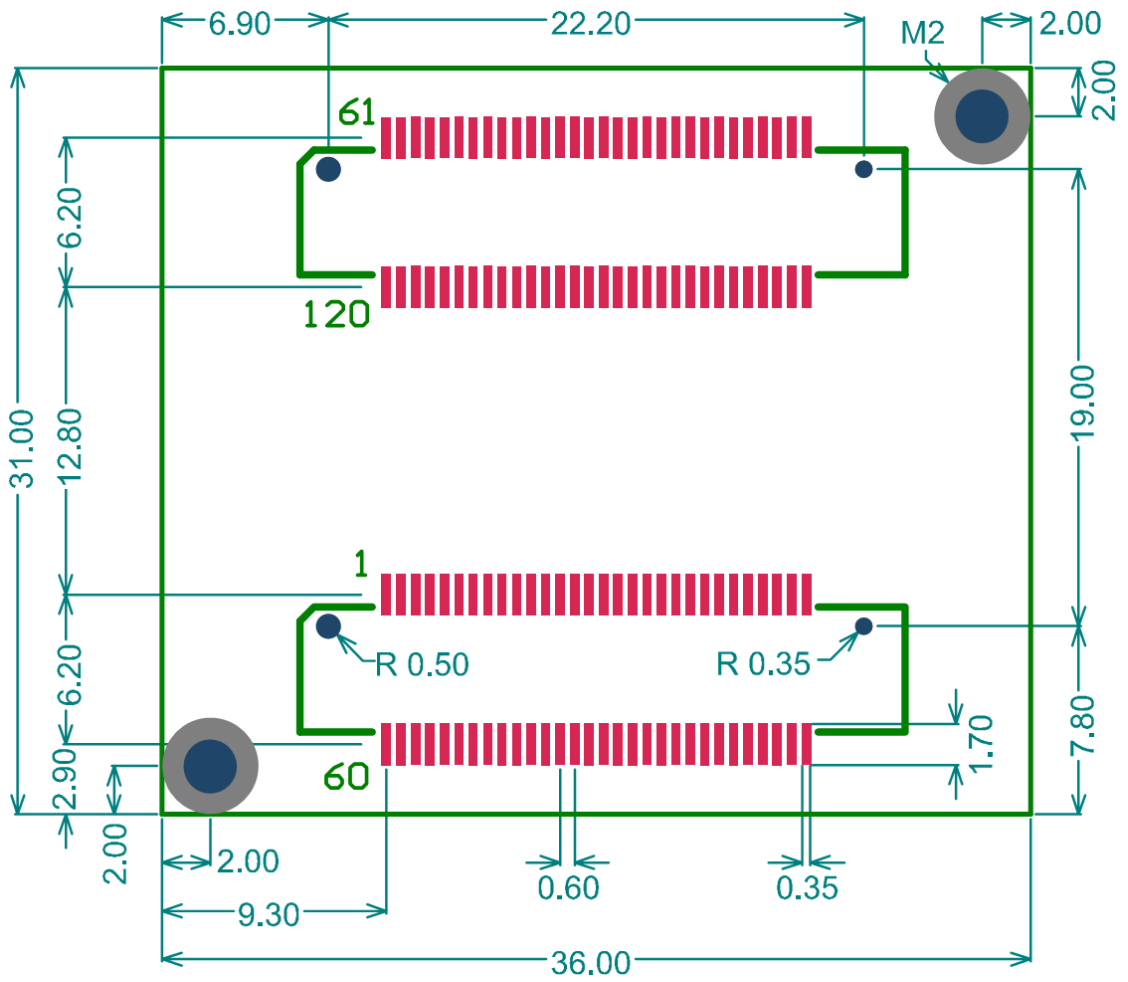

Figure 3-3: Recommended footprint for the Core Module(top view)

3.3 Top Mounted Connector

The optionally mounted connector P4 will not be supported in future versions.

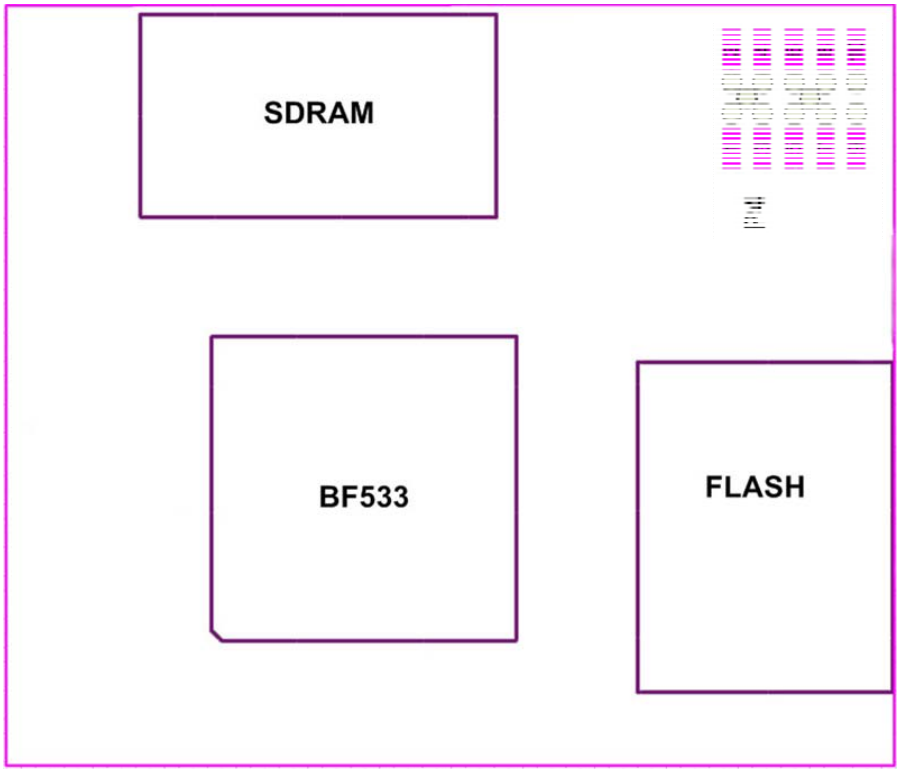

Figure 3-4: P1 - Connector Position (top view)

3.4 Schematic Symbol (Signals of P1 and P2)

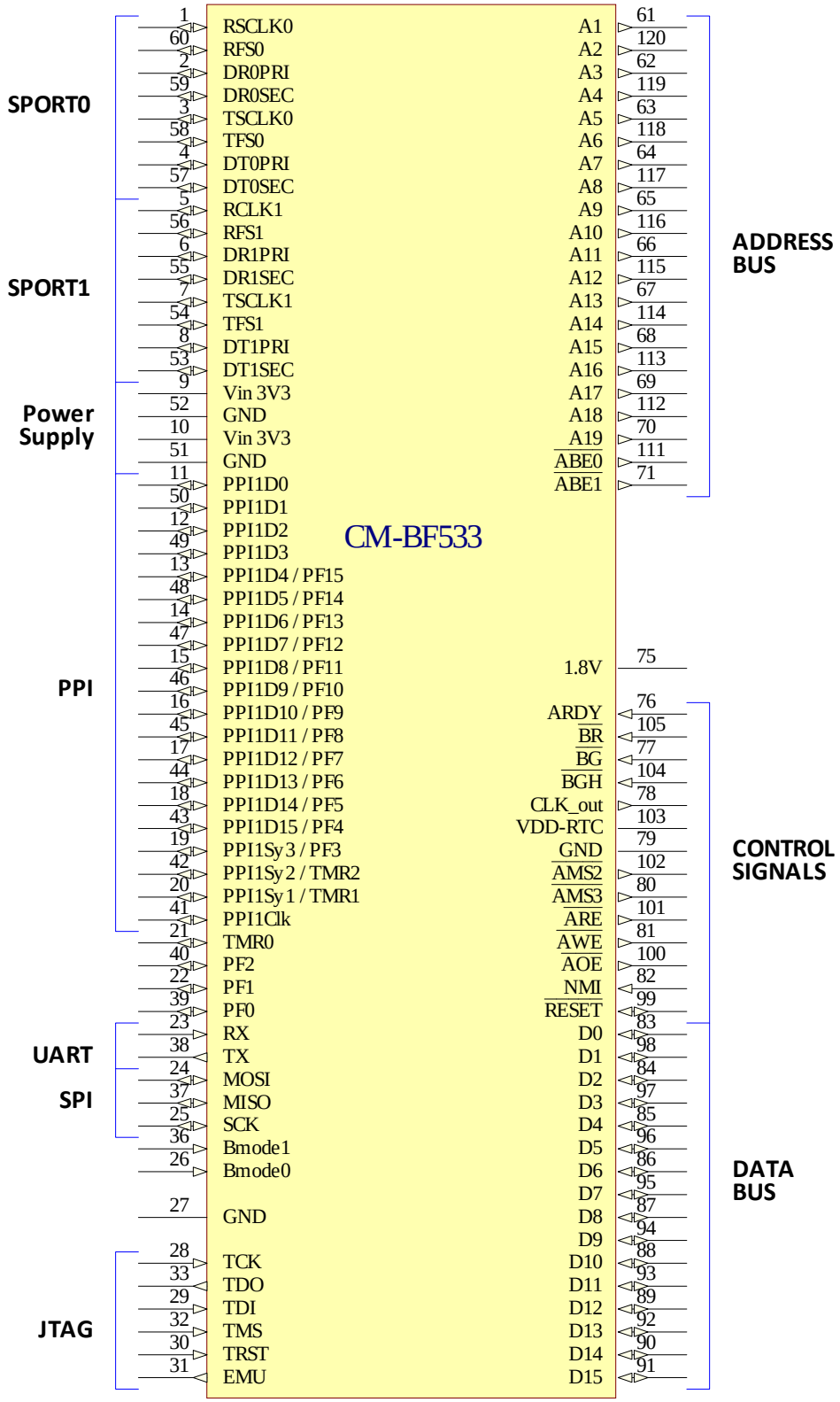

Figure 3-5: Schematic Symbol of Module

3.5 Connectors Pin Assignment P1 – (1-60)

Pin No.	Signal	Signal Type.
1	RSCLK0	I/O
2	DR0PRI	I
3	TSCLK0	I/O
4	DT0PRI	O
5	RSCLK1	I/O
6	DR1PRI	I
7	TSCLK1	I/O
8	DT1PRI	O
9	Vin 3V3	PWR
10	Vin 3V3	PWR
11	PPI1D0	I/O
12	PPI1D2	I/O
13	PF15 / PPI1D4	I/O
14	PF13 / PPI1D6	I/O
15	PF11 / PPI1D8	I/O – 10k pull up
16	PF9 / PPI1D10	I/O
17	PF7 / SPISEL7 / PPI1D12	I/O
18	PF5 / SPISEL5 / PPI1D14	I/O
19	PF3 / SPISEL3 / PPI1Sy3	I/O – 10k pull up
20	TMR1 / PPI1_Sy1	I/O
21	TMR0	I/O
22	PF1 / SPISEL1 / TMRCLK	I/O
23	RX	I – 100k pull up
24	MOSI	I/O
25	SCK	I
26	BMODE0	I – 100k pull down
27	GND	PWR
28	TCK	I – 10k pull up
29	TDI	I – 10k pull up
30	$\overline{\text{TRST}}$	I – 4k7 pull down
31	$\overline{\text{EMU}}$	O
32	TMS	I – 10k pull up
33	TDO	O
34	Disconnected	-
35	Disconnected	-
36	BMODE1	I – 100k pull down
37	MISO	I/O
38	TX	O
39	PF0 / nSPISS	I/O
40	PF2 / SPISEL2	I/O
41	PPI_CLK	I/O
42	TMR2 / PPI1Sy2	I/O
43	PF4 / SPISEL4 / PPI1D15	I/O
44	PF6 / SPISEL6 / PPI1D13	I/O

45	PF8 / PPI1D11	I/O
46	PF10 / PPI1D9	I/O – 10k pull up
47	PF12 / PPI1D7	I/O
48	PF14 / PPI1D5	I/O
49	PPI1D3	I/O
50	PPI1D1	I/O
51	GND	PWR
52	GND	PWR
53	DT1SEC	O
54	TFS1	I/O
55	DR1SEC	I
56	RFS1	I/O
57	DT0SEC	O
58	TFS0	I/O
59	DR0SEC	I
60	RFS0	I/O

Table 3-3: Connector P1 pin assignment

All Pin names of the connectors correspond to the names found in the Blackfin ADSP-BF533 datasheet from Analog Devices.

3.6 Connector Pin Assignment P2 – (61-120)

Pin No.	Signal	IO Type.
61	A1	O
62	A3	O
63	A5	O
64	A7	O
65	A9	O
66	A11	O
67	A13	O
68	A15	O
69	A17	O
70	A19	O
71	ABE1/SDQM1	O
72	N.C.	-
73	N.C.	-
74	N.C.	-
75	N.C.	O
76	ADRY	I – 10k pull up
77	$\overline{BG}$	O
78	CLK_Out	O
79	GND	PWR
80	$\overline{AMS3}$	O
81	$\overline{AWE}$	O
82	NMI	I – 10k pull down
83	D0	I/O
84	D2	I/O
85	D4	I/O
86	D6	I/O
87	D8	I/O
88	D10	I/O
89	D12	I/O
90	D14	I/O
91	D15	I/O
92	D13	I/O
93	D11	I/O
94	D9	I/O
95	D7	I/O
96	D5	I/O
97	D3	I/O
98	D1	I/O
99	$\overline{Reset}$	I – see chapter 3.9
100	$\overline{AOE}$	O
101	$\overline{ARE}$	O
102	$\overline{AMS2}$	O
103	VDD-RTC	PWR
104	$\overline{BGH}$	O

105	$\overline{BR}$	I – 10k pull up
106	N.C.	-
107	N.C.	-
108	N.C.	-
109	N.C.	-
110	N.C.	-
111	ABE0/SDQM0	O
112	A18	O
113	A16	O
114	A14	O
115	A12	O
116	A10	O
117	A8	O
118	A6	O
119	A4	O
120	A2	O

Table 3-4: Connector P2 pin assignment

Non processor Pins:

CLK_OUT: 25MHz buffered output clock of main oscillator. (Pin 78).

All other pins correspond directly to the respective ADSP-BF533 processor pins.

For details about the meaning of the signal names consult the Blackfin ADSP-BF533 datasheet.

3.7 ITU656 Camera Connector P3 (1-22)

The ITU656 connector has been tested only with the OmniVision cameras available in our camera kit Kit-CAM-OV. It is not recommended to use this connector!

Pin No.	Signal	Signal Type.
1	Disconnected	-
2	AGND	PWR
3	SIO_D	I/O
4	AVDD	PWR
5	SIO_C	I
6	RESET	I
7	VSYNC	O
8	PWDN	I
9	HREF	O
10	DVDD	PWR
11	DOVDD	PWR
12	D7	O
13	XClk	I
14	D6	O

15	DGND	PWR
16	D5	O
17	PCLK	O
18	D4	O
19	D0	O
20	D3	O
21	D1	O
22	D2	O
23	N.C.	-
24	N.C.	-

Table 3-5: Connector P3 pin assignment

3.8 Connector P4 (1-10)

The top optionally mounted connector P4 can be used as a stand-alone connector for a system requiring only power supply and one or two communication ports (UART and SPI)

Pin No.	Signal	Signal Type.
1	RX	I
2	TX	O
3	MOSI	I/O
4	GND	PWR
5	SCK	I/O
6	PF0	I/O
7	PF2	I/O
8	MISO	I/O
9	3V3	PWR
10	PF1	I/O

Table 3-6: Connector P4 pin assignment

3.9 Reset circuit

The reset of the flash and the processor are connected to a power monitoring IC. The output can be used as power on reset for external devices, see Figure 3-6.

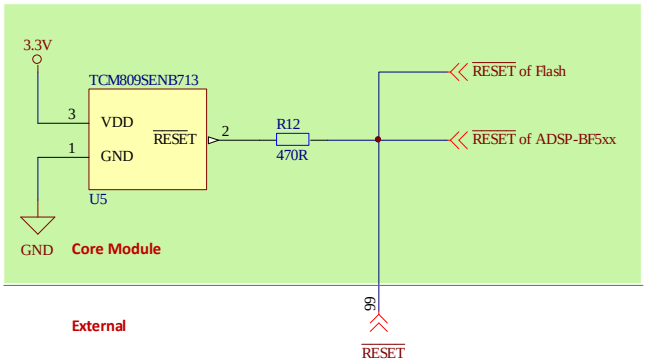

Figure 3-6: Schematic of reset circuit on the Core Module

4 Test Points

4.1 Footprint – Test Points

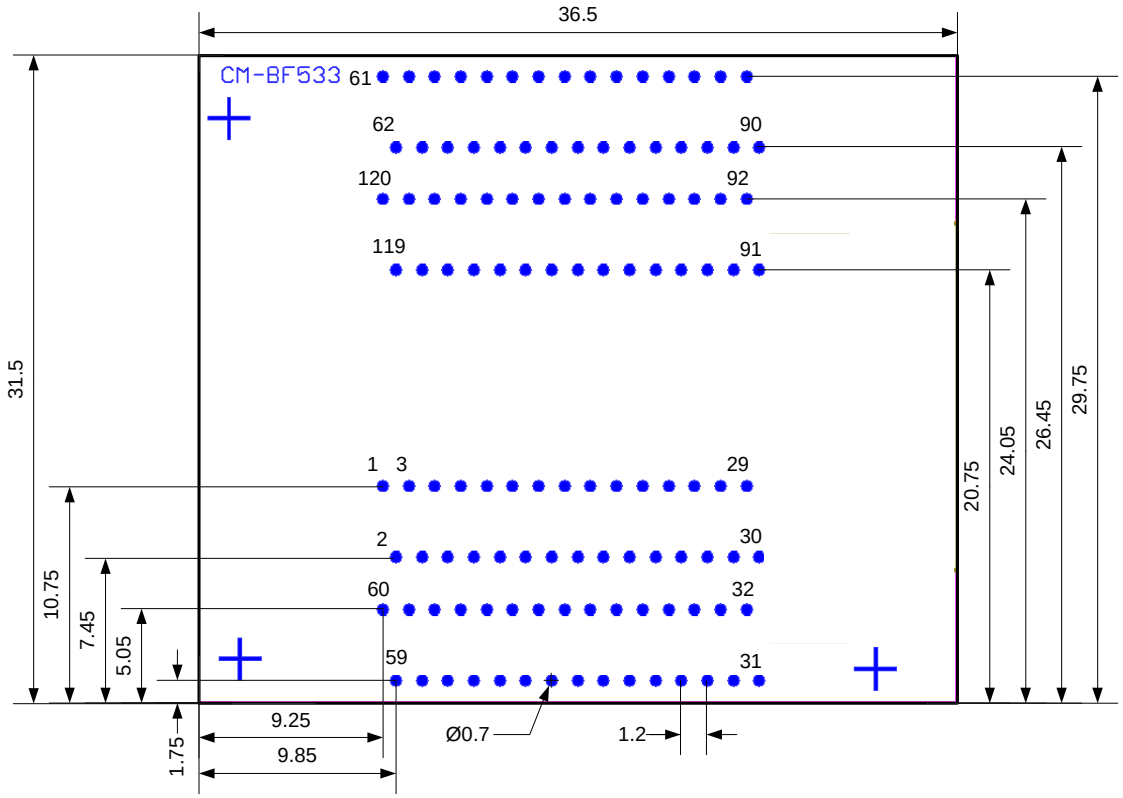

Figure 4-1: Test Points of the Core Module

5 Application Examples

5.1 Sample Application

In this minimum configuration the CM-BF533 is used as a high performance SPI-based co-processor module.

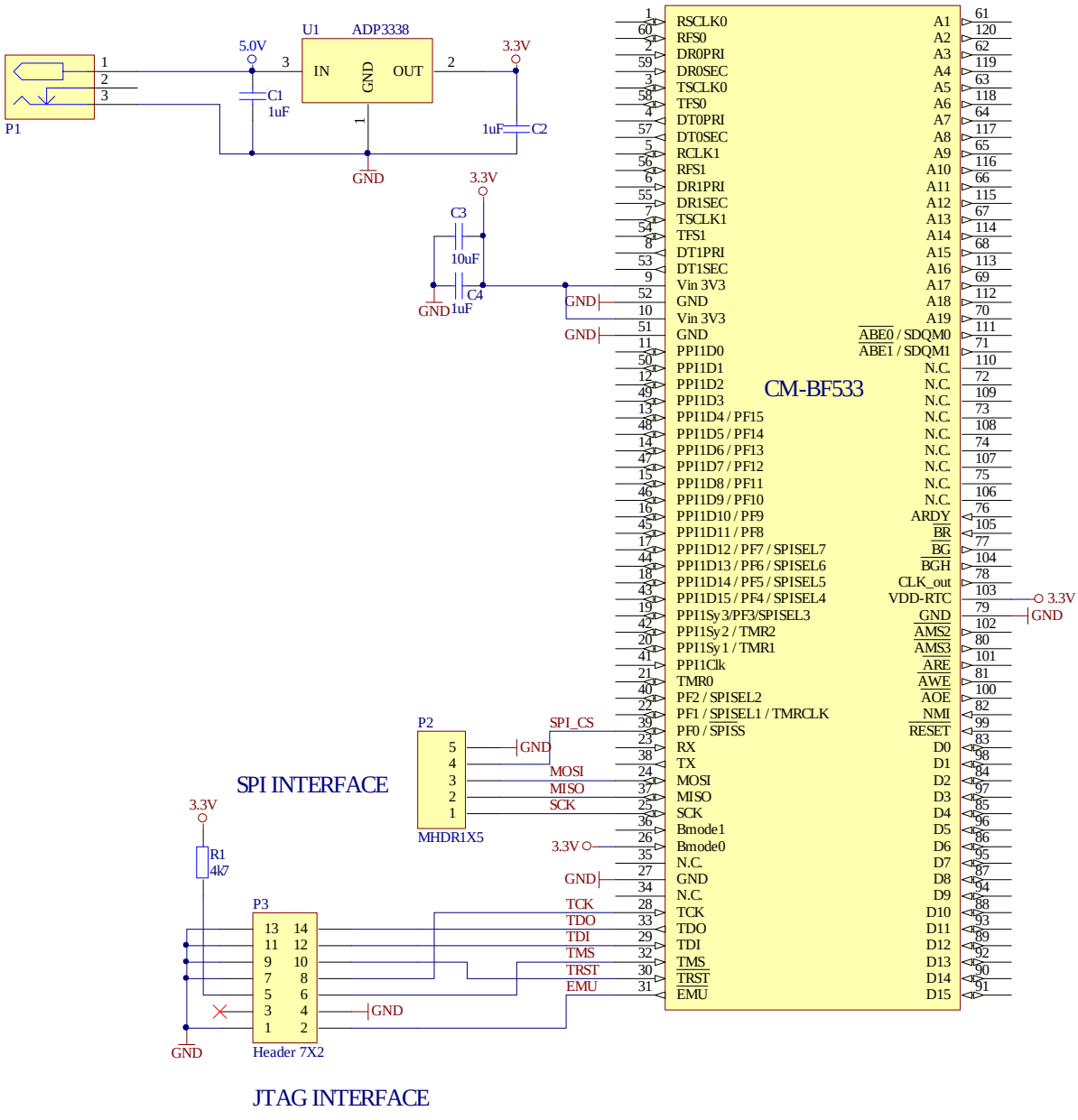

Figure 5-1: Minimum Configuration with SPI and JTAG Connector

5.2 Mini Camera System

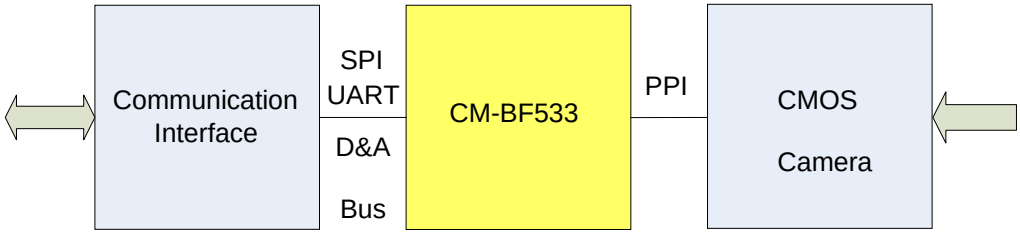

Figure 5-2: Block Diagram – Mini Camera Module

5.3 Generic Signal Processing System

Figure 5-3: Block Diagram – Analog Signal Processing Module

5.4 Coprocessor Application

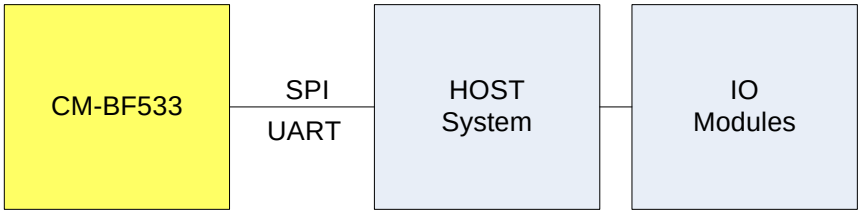

Figure 5-4: Block Diagram – Coprocessor Module

5.5 Digital Video System

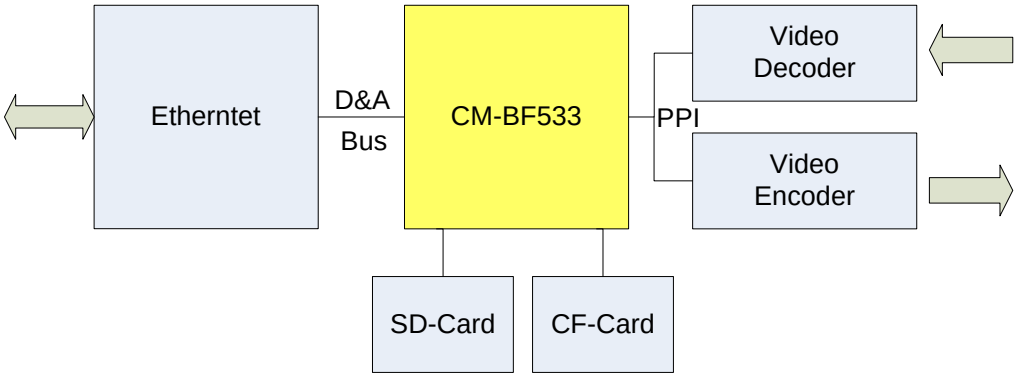

Figure 5-5: Block Diagram: Digital Video System

5.6 Design Services

Bluetechnix offers custom design services and software development.

6 Software Support

6.1 BLACKSheep

The Core Module is delivered with a pre-flashed basic version of the BLACKSheep VDK multithreaded framework. It contains a boot-loader for flashing the Core Module via the serial port.

Please consult the software development documents.

6.2 uClinux

The Core Module is fully supported by the open source platform at http://blackfin.uclinux.org. Since the Core Modules are pre-flashed with BLACKSheep you have to flash uBoot first. To flash uBoot you can use the BLACKSheep boot-loader.

7 Anomalies

For the latest information regarding anomalies for this product, please consult the product home page:

http://www.bluetechnix.com/goto/cm-bf533

8 Production Report for CM-BF533 (100-1203)

Version	Component	Type
V2.0.3	Processor	ADSP-BF533SKBCZ600 (Rev 0.4)
	RAM	MT48LC16M16A2BG
	FLASH	PC28F320J3D-75
V2.0.4	Processor	ADSP-BF533SKBCZ600 (Rev 0.5)
	RAM	MT48LC16M16A2BG-75IT
	FLASH	PC28F320J3D-75

Table 8-1: Production Report CM-BF533

9 Product Changes

For the latest product change information please consult the product web-page at:

http://www.bluetechnix.com/goto/cm-bf533

Version	Changes
1.3 to 2.0	RoHS compliant
1.2 to 1.3	Pin 75 (1.8V) in a future revision not supported
	Crystal frequency (27MHz to 25MHz)
	Boot mode default settings from 01 to 00

Table 9-1: Product Changes

10 Document Revision History

Version	Date	Document Revision
11	2010-01-26	Redesign of Manual
10	2008-12-03	Pull up/down information added Reset circuit added
9	2008-09-03	Footprint and mechanical drawings updated
8	2008-08-12	English checked for grammar, spelling and clarity
7	2008-01-04	Delete unclear part
6	2007-04-05	BGA option removed
5	2007-03-25	Bugs, Product Changes and Revision Tables updated
4	2006	Several minor Changes
3	2005-12-22	New version of the document –CM-BF533 V2.0
	2005-12-20	Updated Figures and tables
	2005-10-13	Modifications on Table 2-3: EMU and TMS Signal type changed. Signal names of PPI and timer pins changed.
2	2005-01-09	Memory Map added
1	2004-08-28	First release V1.0 of the Document

Table 10-1: Revision History

A List of Figures and Tables

Figures

Figure 1-1: Main Components of the CM-BF533 module 8
Figure 2-1: Detailed Block Diagram 10
Figure 3-1: Mechanical outline and Bottom Connectors (Top-View) 12
Figure 3-2: Side View with connectors mounted 12
Figure 3-3: Recommended footprint for the Core Module(**top view**) 13
Figure 3-4: P1 - Connector Position (**top view**) 14
Figure 3-5: Schematic Symbol of Module 15
Figure 3-6: Schematic of reset circuit on the Core Module 20
Figure 4-1: Test Points of the Core Module 21
Figure 5-1: Minimum Configuration with SPI and JTAG Connector 22
Figure 5-2: Block Diagram – Mini Camera Module 23
Figure 5-3: Block Diagram – Analog Signal Processing Module 23
Figure 5-4: Block Diagram – Coprocessor Module 23
Figure 5-5: Block Diagram: Digital Video System 23

Tables

Table 2-1: Memory Map 11
Table 3-1: Module connector types 13
Table 3-2: Baseboard connector types 13
Table 3-3: Connector P1 pin assignment 17
Table 3-4: Connector P2 pin assignment 19
Table 3-5: Connector P3 pin assignment 20
Table 3-6: Connector P4 pin assignment 20
Table 8-1: Production Report CM-BF533 24
Table 9-1: Product Changes 25
Table 10-1: Revision History 25